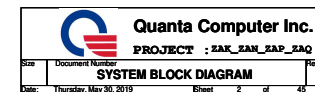


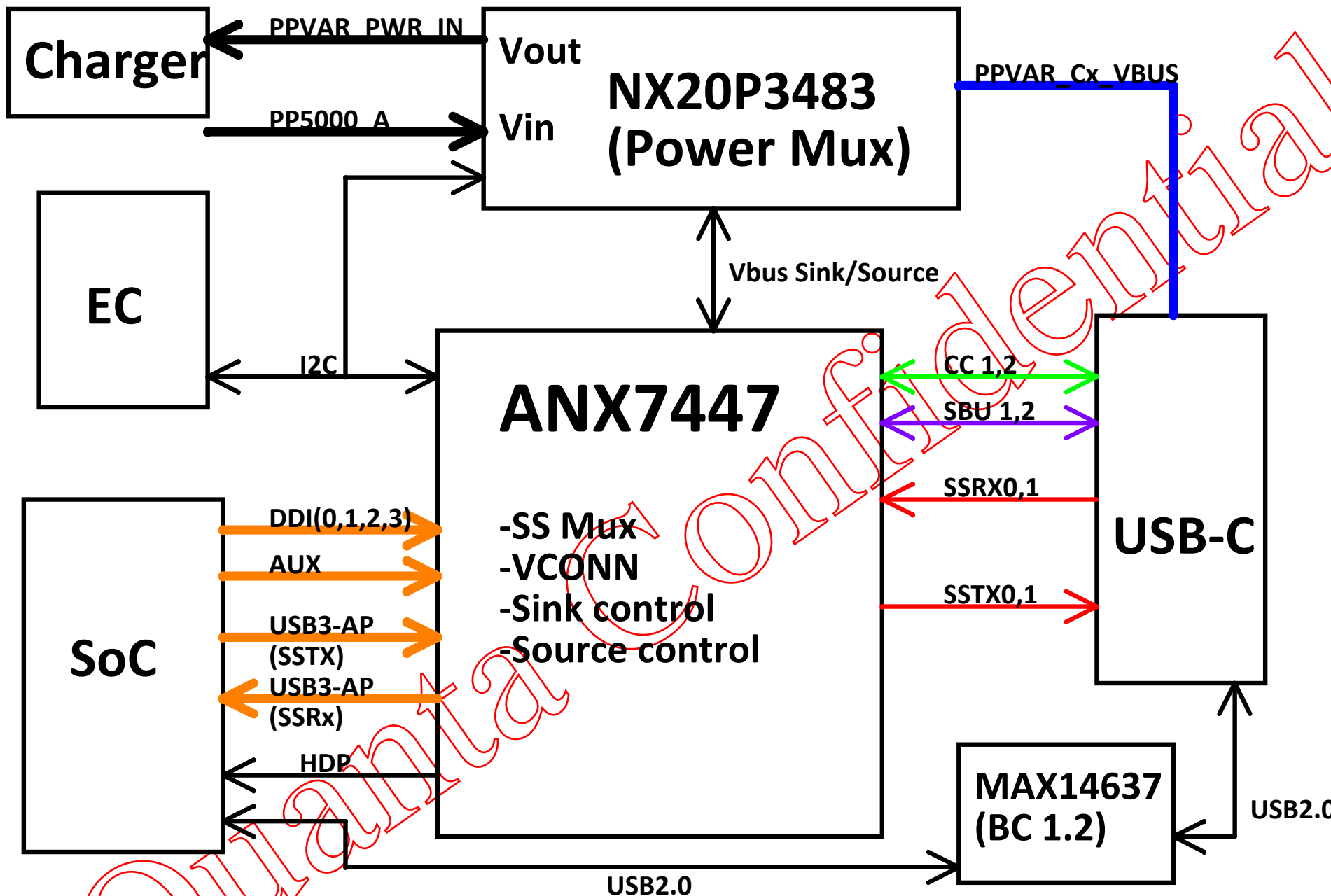
SCH: 650-01771-03-SCH
ASSY:650-01771-03
PCB: 651-01771-03

SHEET NO.	SHEET NAME
1	TABLE OF CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	USB TYPE-C BLOCK DIAGRAM
4	POWER TREE
5	I2C MAP
6	SOC DRAM I/F
7	SOC EDP/MIPI/DDI
8	SOC PCIE/USB/SATA
9	SOC AUDIO/EMMC/LPC/SPI
10	SOC I2C/CNVI/UART/SPI
11	SOC PMU/RTC/SVID/THERMAL/MISC
12	SOC JTAG/GPIO/ITP
13	SOC GROUND
14	SOC POWER
15	SOC DECOUPLING
16	MEMORY CH 00/01 LPDDR4
17	MEMORY CH 10/11 LPDDR4
18	EC-NUVOTON
19	SPI ROM
20	MIPI60 DEBUG HEADER
21	H1 SECURE MICROCONTROLLER
22	SERVO
23	eMMC/SD
24	AUDIO
25	KB, TP, PEN
26	LID: eDS, CAM, TOUCH, SENSOR
27	SENSOR: COMPASS, GYRO
28	WIFI/BT CONNECTOR
29	USB C TCPC/MUX
30	USB A CONNECTIONS (MLB)

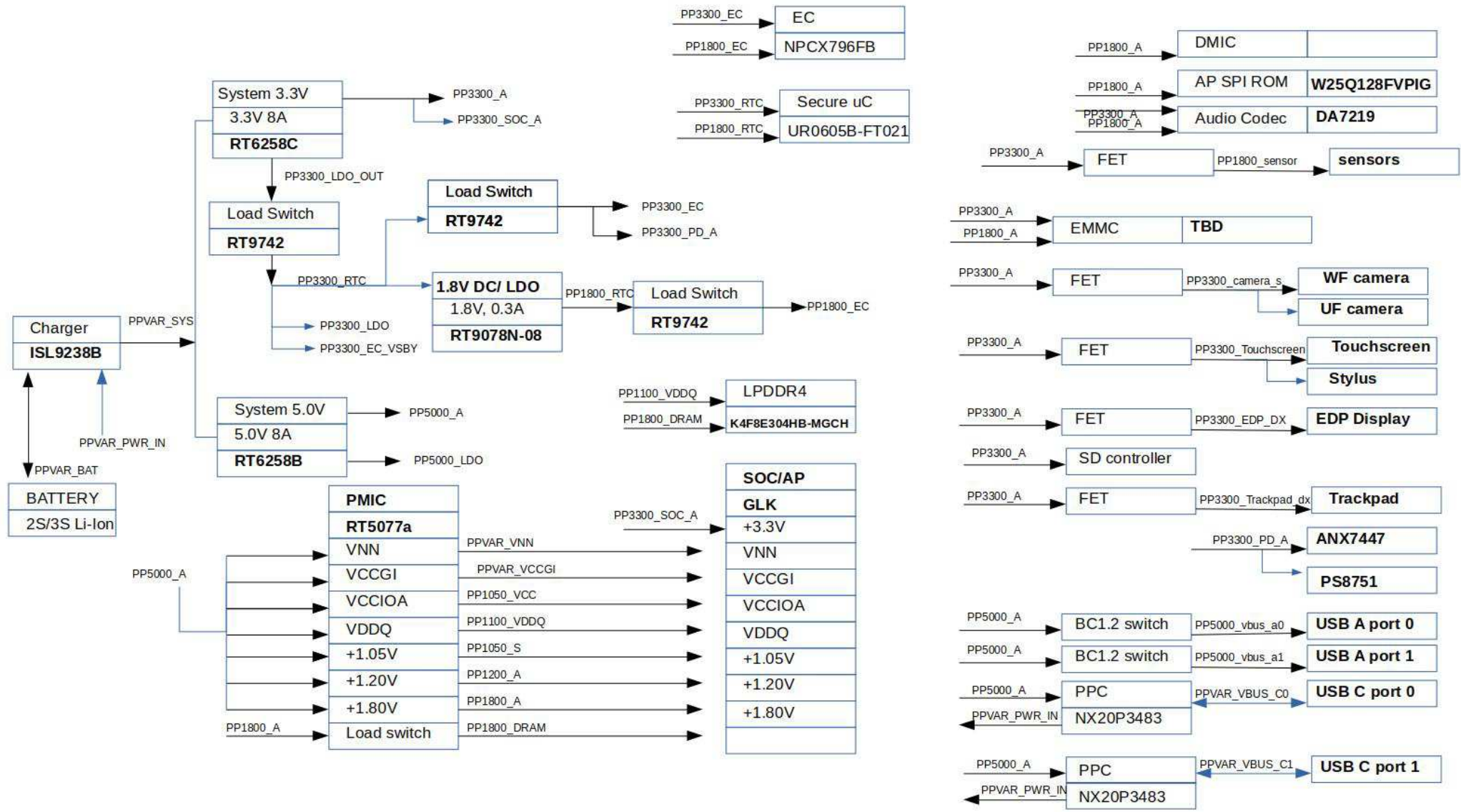
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Apr, 24, 2018

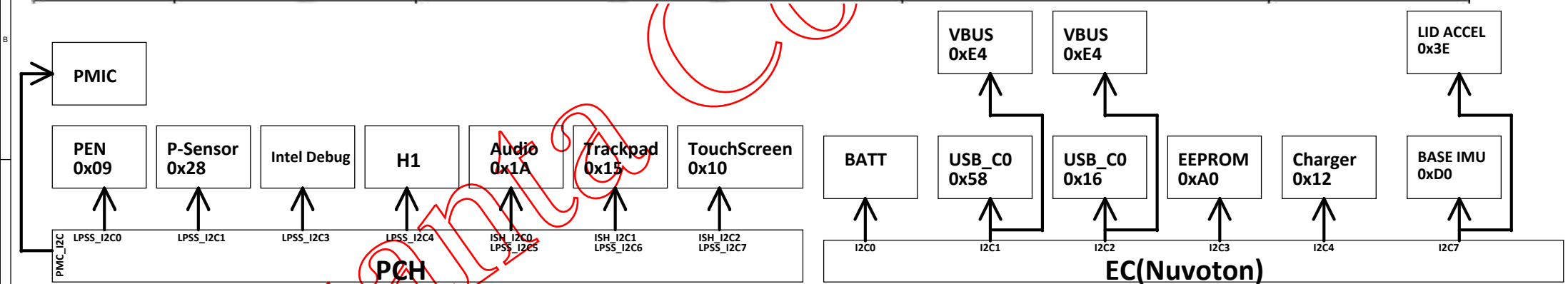




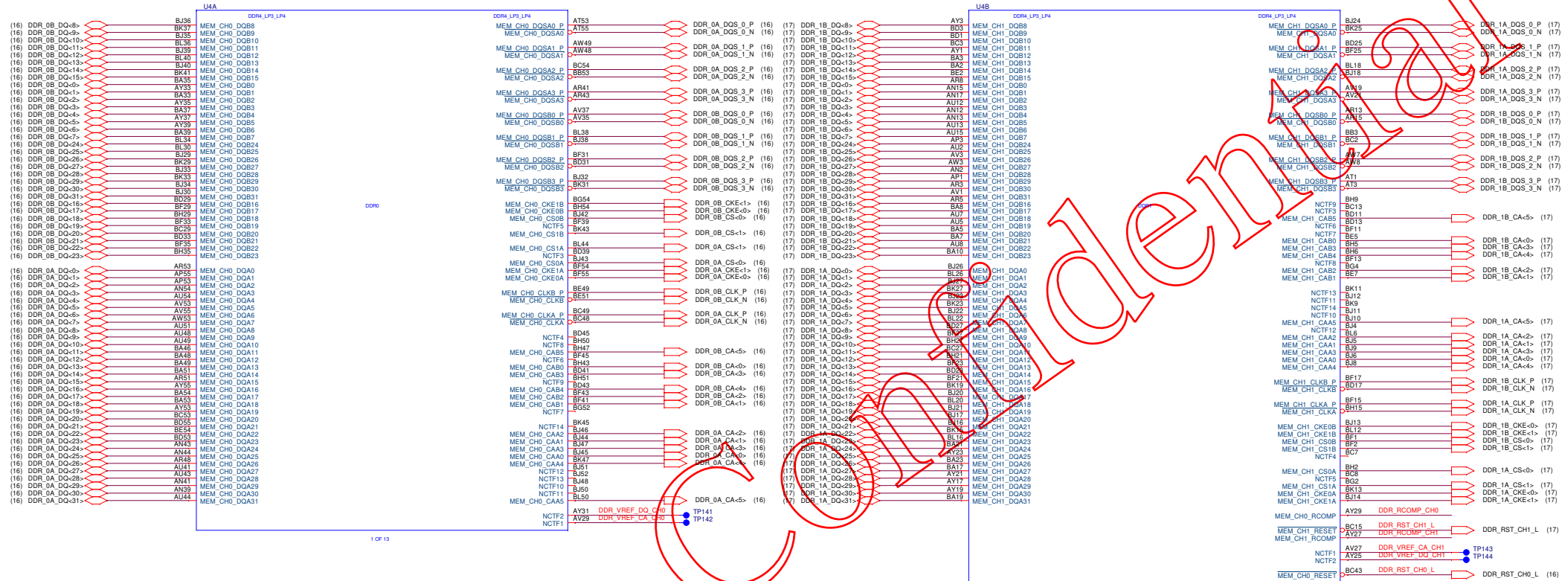
Power Tree



Master	Port	Net Name	Slave Device(S)	Speed
EC	I2C0 0	EC I2C BATTERY 3V3	BATTERY (TBD)	100KHZ
EC	I2C1 0	EC I2C USB C0 MUX	ANX7447, NX20P3483 <i>Check subboard</i>	100KHZ
EC	I2C2 0	EC I2C USB C1 MUX		100KHZ
EC	I2C3 0	EC I2C EEPROM SCL	M34E02	100KHZ
EC	I2C4 1	EC I2C CHARGER 3V3	ISL9238B	100KHZ
EC	I2C5 0	-		
EC	I2C7 0	EC I2C SENSOR U	LSM6DS3TR, LIS2MDLTR	400KHZ
AP	LPSS I2C0	PCH I2C PEN	STYLUS (TBD)	400KHZ
AP	LPSS I2C1	PCH I2C P SENSOR	TBD	100KHZ
AP	LPSS I2C2	-		
AP	LPSS I2C3	DBG PCH I2C	TBD	TBD
AP	LPSS I2C4	PCH I2C H1	H1 (not used)	100KHZ
AP	LPSS I2C5	PCH I2C AUDIO	DA7219	100KHZ
AP	LPSS I2C6	PCH I2C TRACKPAD	TRACKPAD (TBD)	100KHZ
AP	LPSS I2C7	PCH I2C TOUCHSCREEN	TOUCHSCREEN (TBD)	100KHZ
AP	PMC I2C	PCH PMIC I2C	RT5077A	100KHZ

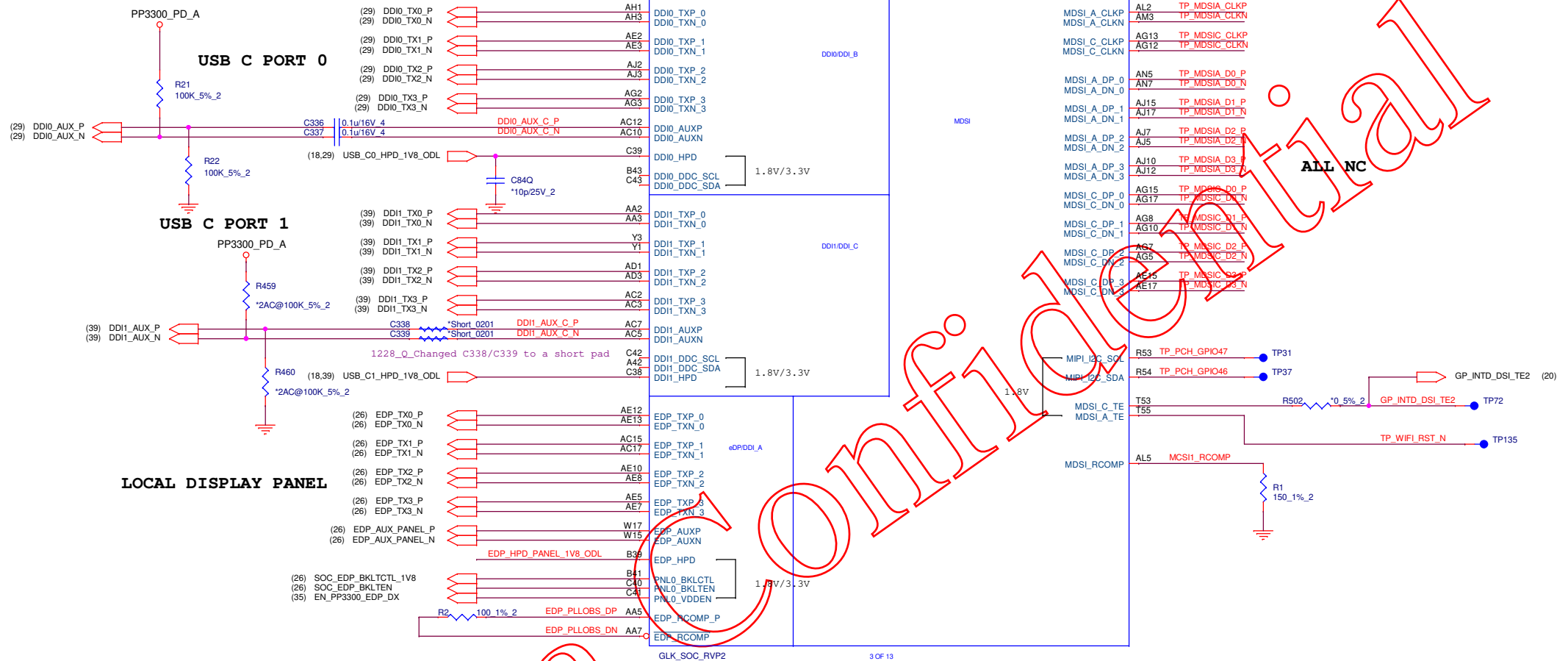


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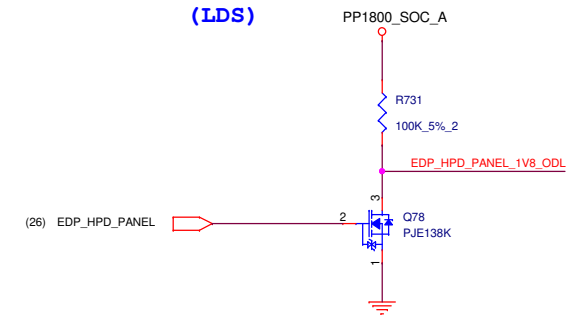


Gemini lake (DISPLAY, eDP)

(CPU)



(LDS)

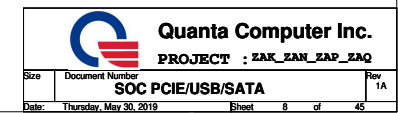


Quanta Computer Inc.

PROJECT : ZAK_ZAN_ZAP_ZAQ

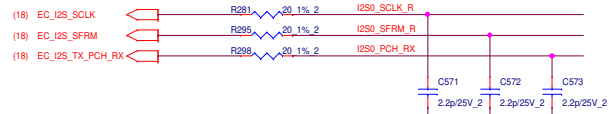
Size	Document Number	Rev
	SOC EDP/MIPI/DDI	1A
Date:	Thursday, May 30, 2019	Sheet 7 of 45

(CPU)

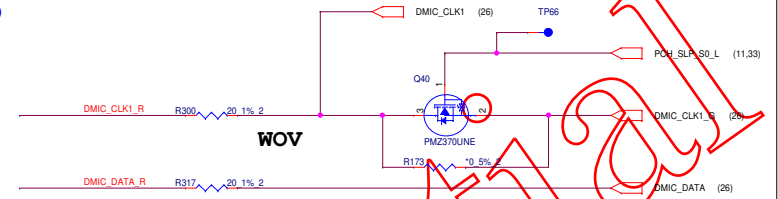


Gemini lake (EMMC/LPC/I2C/GPIO/HDA)

(CPU)



(MIC)



(CPU)

TO-EC

SPEAKER AMP

HEADPHONE

DMIC'S

PP1800_SOC_A

(23) EMMC_RCLK

(40) DMIC_CAM2_DATA

(23) EMMC_CLK

(23) EMMC_DAT0

(23) EMMC_DAT1

(23) EMMC_DAT2

(23) EMMC_DAT3

(23) EMMC_DAT4

(23) EMMC_DAT5

(23) EMMC_DAT6

(23) EMMC_DAT7

(23) EMMC_CMD

(23) EMMC_RST_ODL

TEST POINTS ON EMMC CLOSE TO SOC

TP70

TP53

TP54

TP57

TP59

(38) LTE_OFF_ODL

(24) I2S_SCLK_HP

(24) I2S_SFRM_HP

(24) I2S_PCH_RX_HP_TX

(24) I2S_PCH_TX_HP_RX

(24) I2S_MCLK_HP

(26,40) DMIC_CLK2

R282 4.7k 5% 2

R590 100k 1% 6

TP44

TP41

TP42

TP43

TP40

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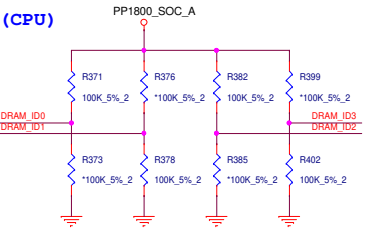
TP259

TP260

TP261

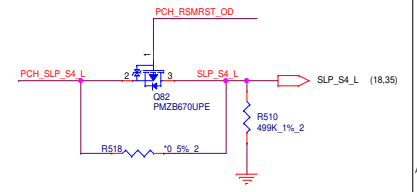
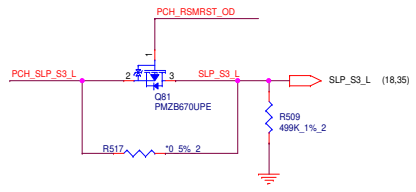
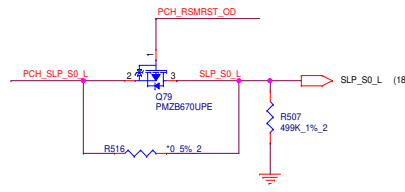
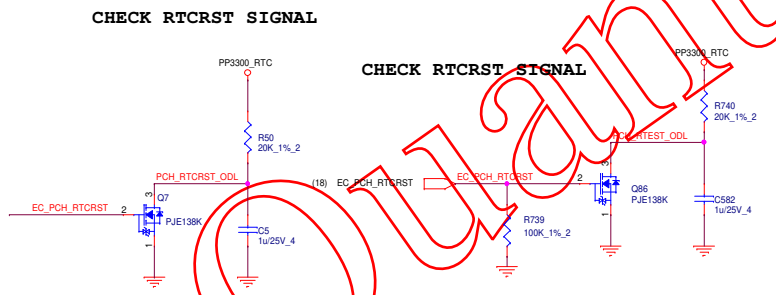
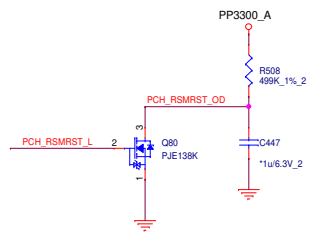
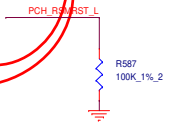
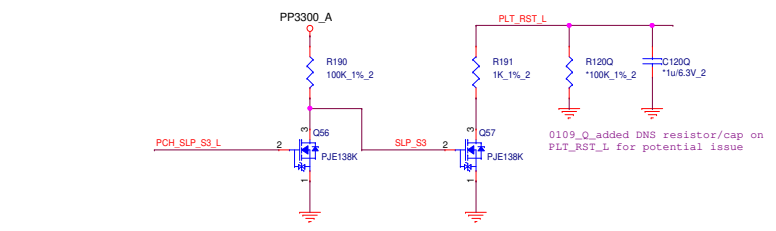
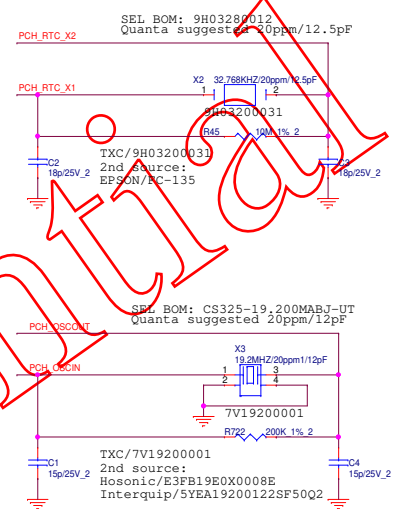
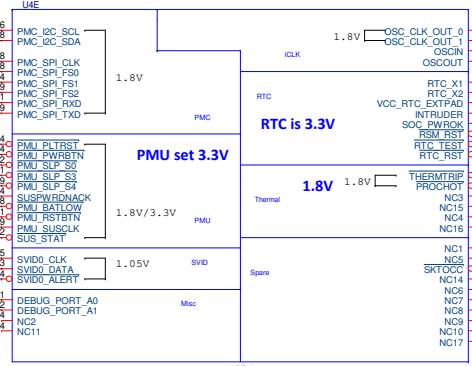
TP262

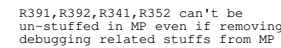
TP263




Vendor	Dram PartNumber	RAM ID	Memory	Rank Density	Dual Rank
Micron	MT53B256M32D1NP-062	0 (0000)	4GiB	8Gb	N
Hynix	H9HCNNN8KUMLR-NME	0 (0000)	4GiB	8Gb	N
Samsung	K4F8E304HB-MGCI	0 (0000)	4GiB	8Gb	N
Nanya	NT6AN256T32AV-I2	0 (0000)	4GiB	8Gb	N
Micron	MT53E512M32D2NP-046	1 (0001)	8GiB	16Gb	N
Samsung	K4F6E354HM-MGCI	1 (0001)	8GiB	16Gb	N
Kingston	B5116PC2WDGPKR	1 (0001)	8GiB	16Gb	N
Micron	MT53B512M32D2NP-062	2 (0010)	8GiB	8Gb	Y
Hynix	H9HCNNNBPUMLHR-NME	2 (0010)	8GiB	8Gb	Y
Samsung	K4F6E304HB-MGCI	2 (0010)	8GiB	8Gb	Y

Gemini lake (PMU/PMIC/RTC)

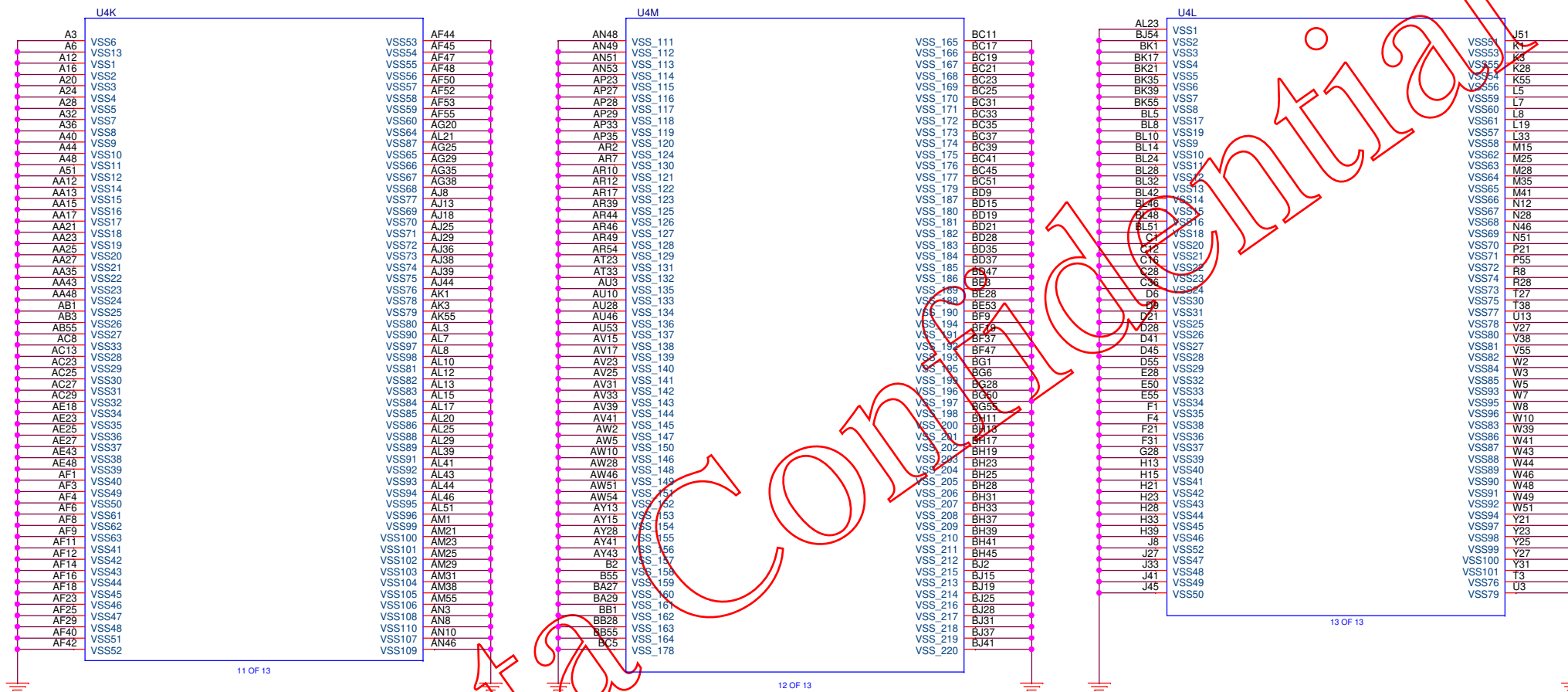




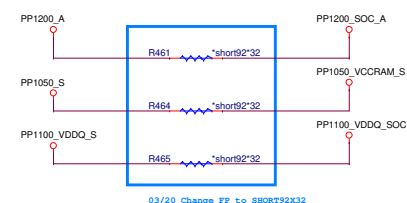
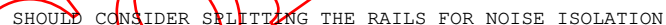
 Quanta Computer Inc. PROJECT : ZAK_ZAN_ZAP_ZAQ		
Size	Document Number	Rev
	SOC JTAG/GPIO/ITP	1A
Date:	Thursday, May 30, 2019	Sheet 12 of 45

(CPU)

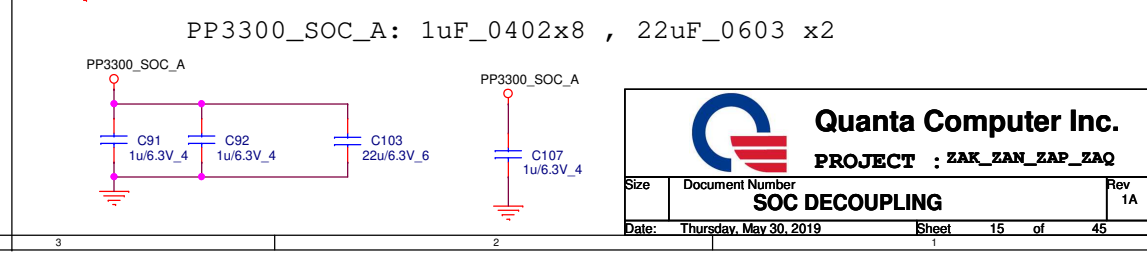
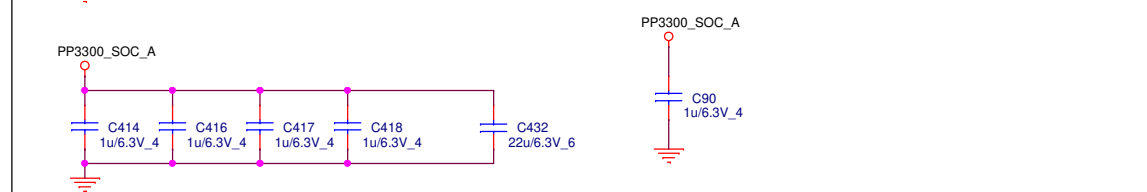
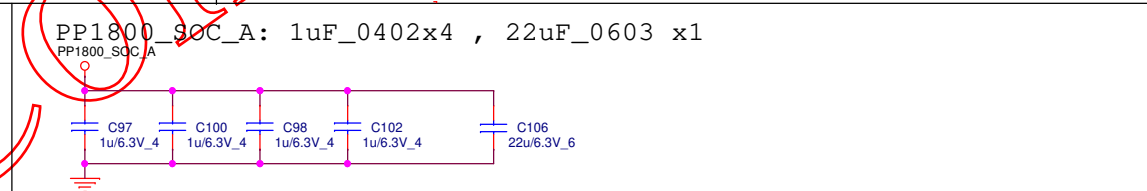
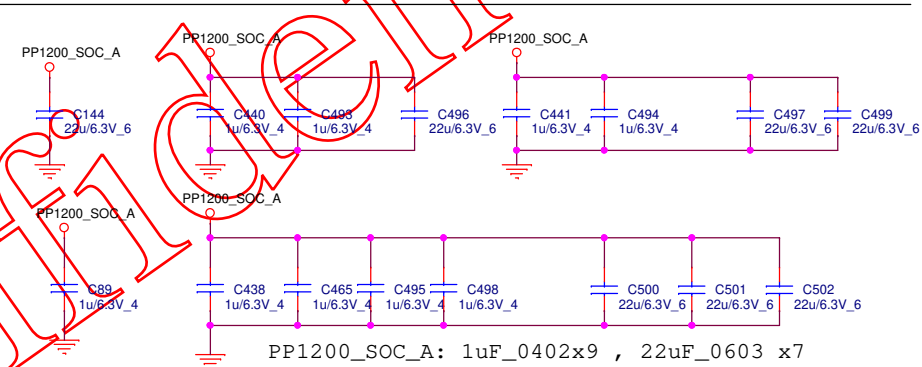
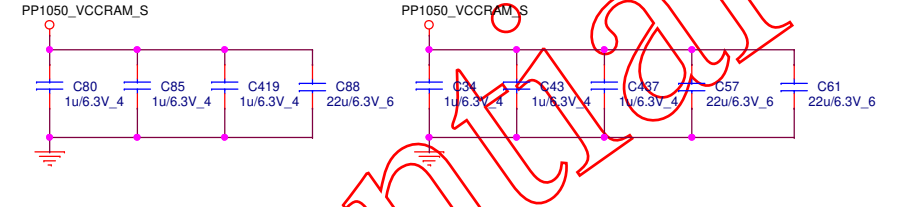
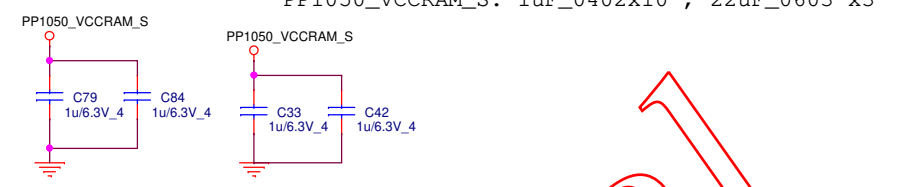
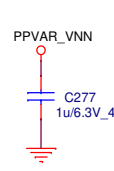
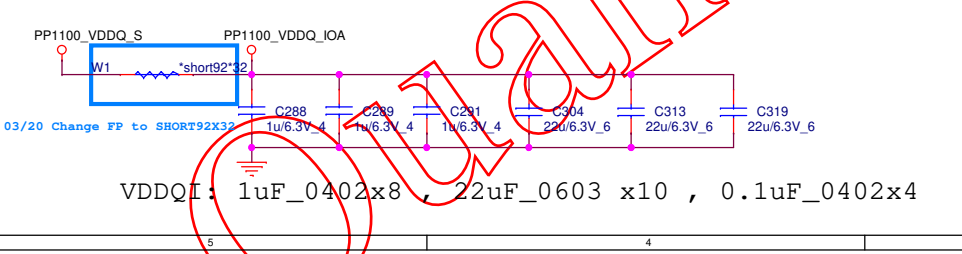
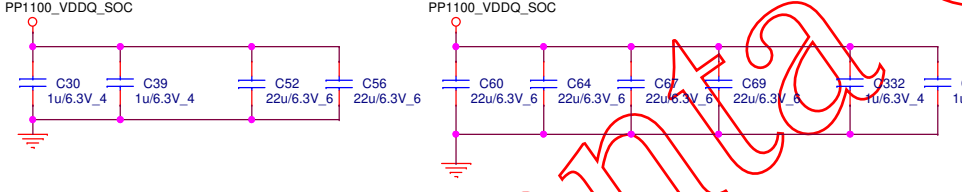
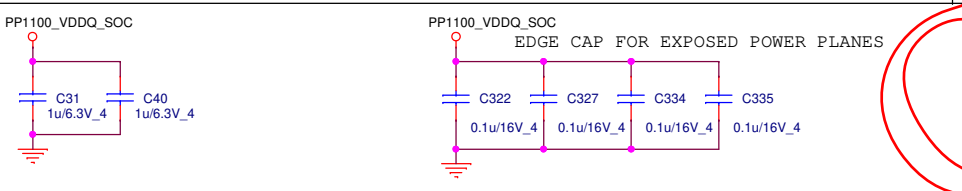
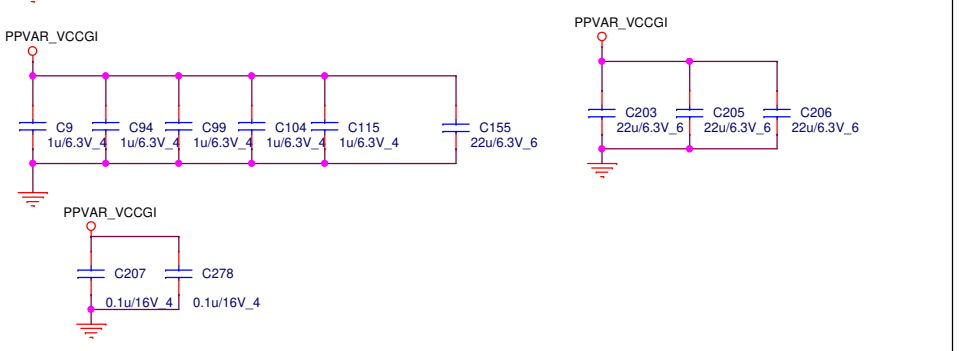
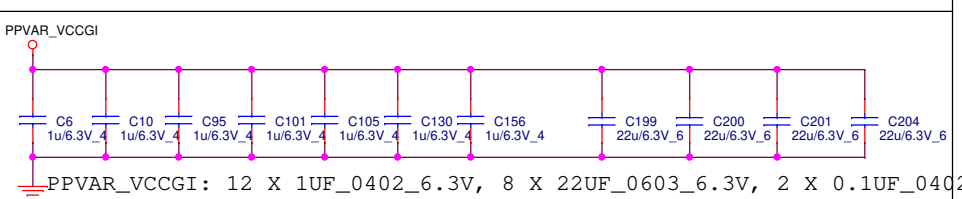
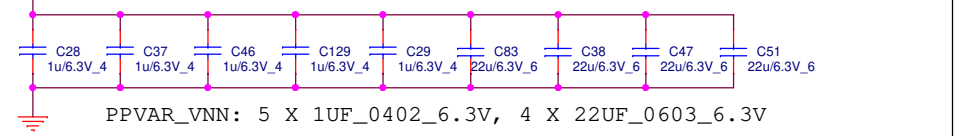
GLK ULT (GND)



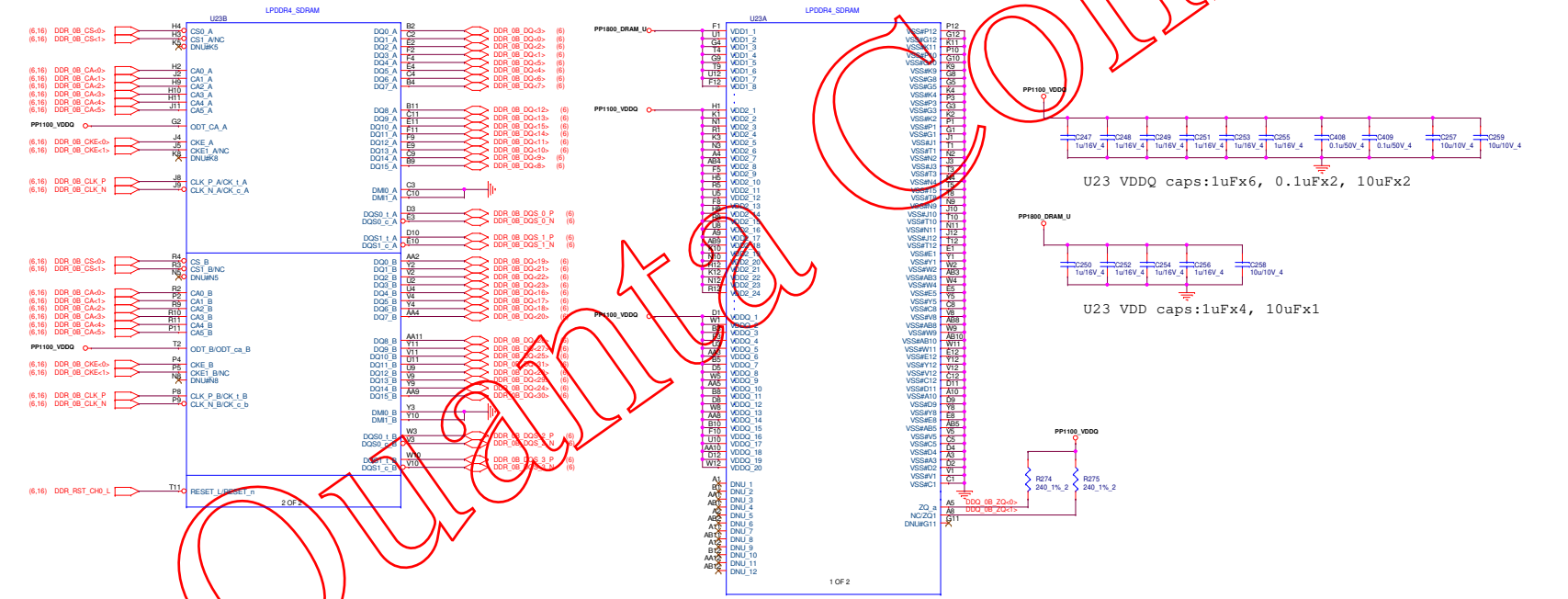
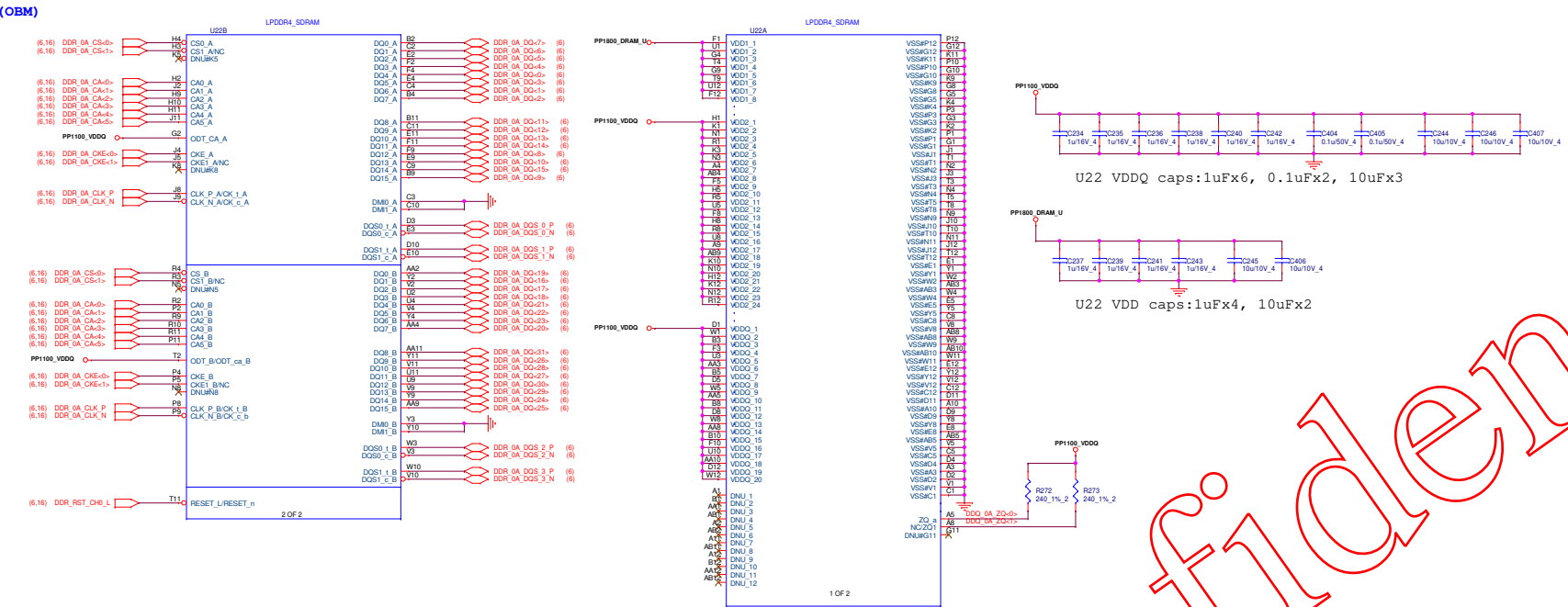
Gemini (POWER)

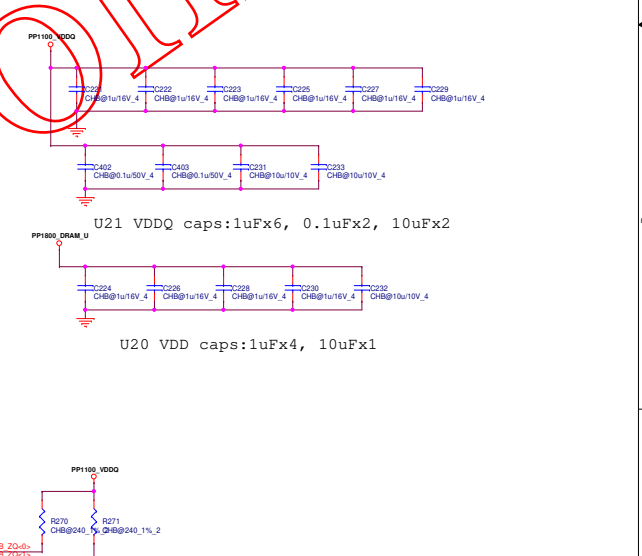
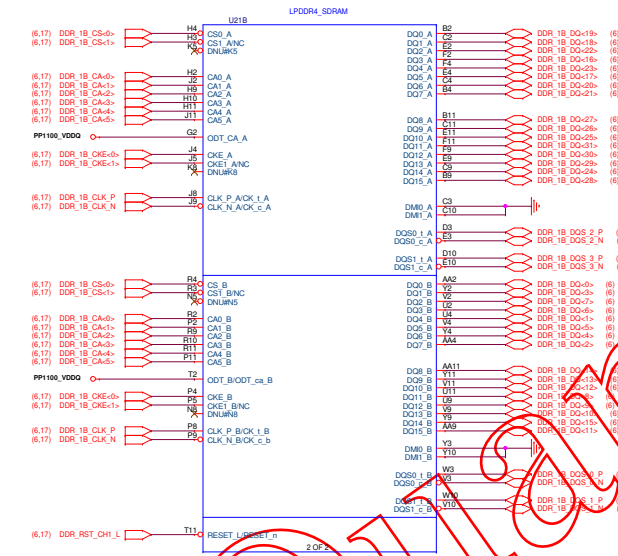
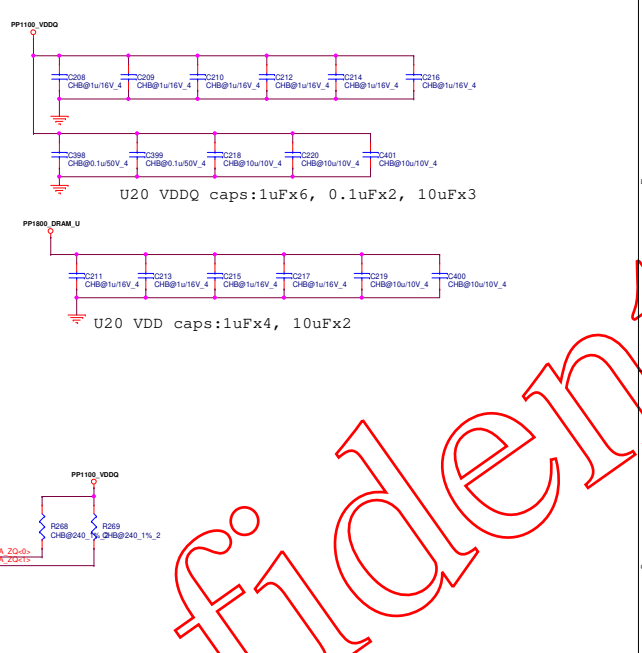
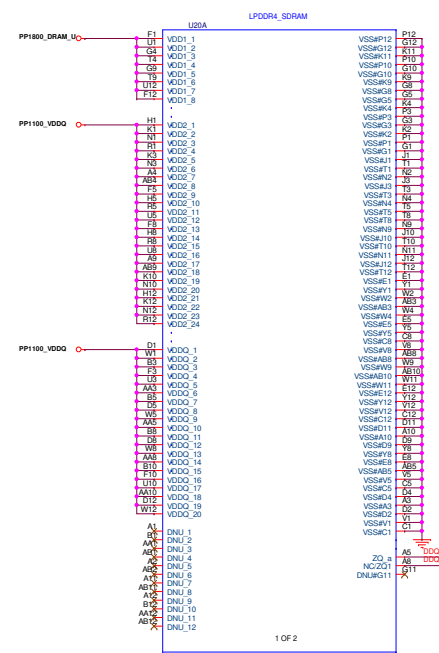
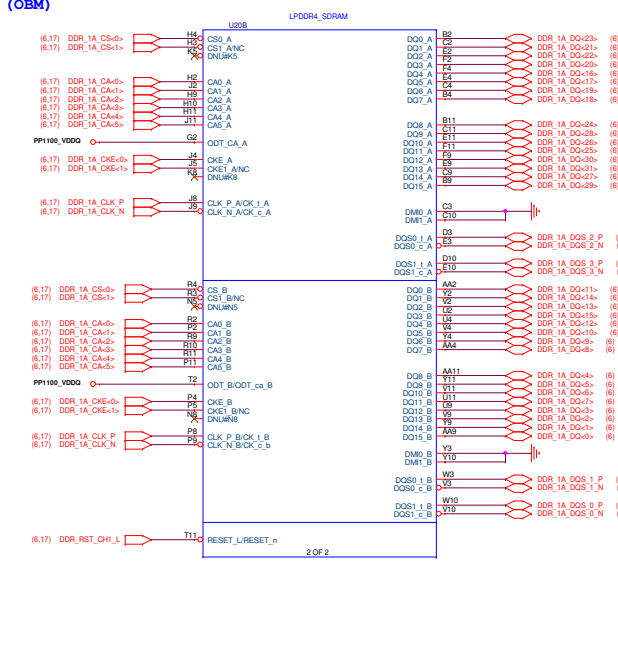


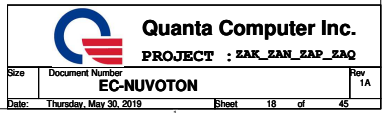
(CPU)
PPVAR_VNN
DECOUPLING VALUES AND NUMBER BASED ON THE REFERENCE DOC



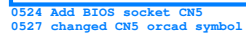
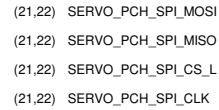
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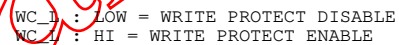


- (9) PCH_SPI_MOSI
- (9) PCH_SPI_MISO_R
- (9) PCH_SPI_CS0_L
- (9) PCH_SPI_CLK



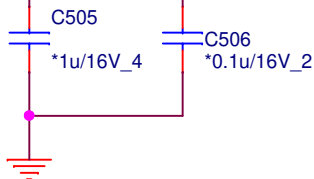
(19,21) H1_AP_FLASH_SEL

SKU EEPROM



(INT)

PP1800_A

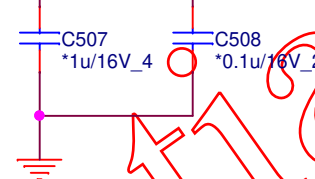


LAYOUT NOTE: PLACING THE SERIAL R'S WITHIN 1 " OF THE DEBUG CONNECTOR

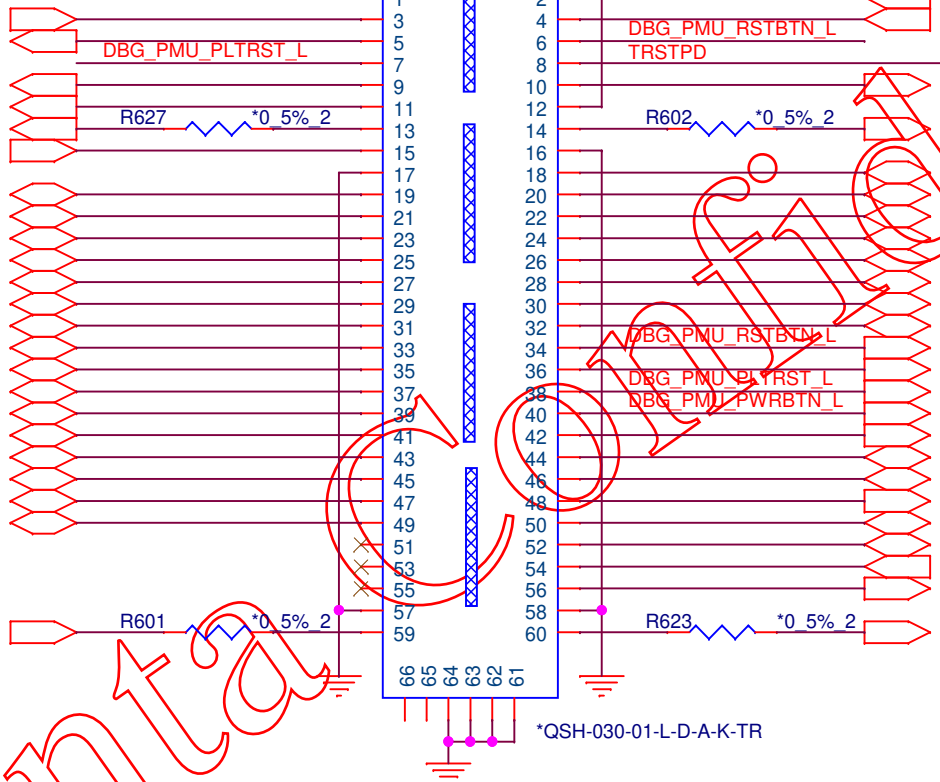
PP1800_A

PP1800_A

PP1800_A



- (12) TCK
- (12) TDI
- (12) TRST_L
- (12) CX_PRDY_L
- (12) DBG_PTI_CLK0
- (7) GP_INTD_DSI_TE2
- (12) DBG_PTI_DATA_0
- (12) DBG_PTI_DATA_1
- (12) DBG_PTI_DATA_2
- (12) DBG_PTI_DATA_3
- (12) DBG_PTI_DATA_4
- (12) DBG_PTI_DATA_5
- (12) DBG_PTI_DATA_6
- (12) DBG_PTI_DATA_7
- (12) DBG_PTI_DATA_8
- (12) DBG_PTI_DATA_9
- (12) DBG_PTI_DATA_10
- (12) DBG_PTI_DATA_11
- (12) DBG_PTI_DATA_12
- (12) DBG_PTI_DATA_13
- (12) DBG_PTI_DATA_14
- (12) DBG_PTI_DATA_15



- TMS (12)
- TDO (12)
- CX_FREQ_L (12)
- DBG_PTI_CLK2 (12)
- DBG_PTI_DATA_16 (12)
- DBG_PTI_DATA_17 (12)
- DBG_PTI_DATA_18 (12)
- DBG_PTI_DATA_19 (12)
- DBG_PTI_DATA_20 (12)
- DBG_PTI_DATA_21 (12)
- DBG_PTI_DATA_22 (12)
- DBG_PTI_DATA_23 (12)
- DBG_PMI_RSTBTN_L (12)
- DBG_PMI_PLTRST_L (12)
- DBG_PMI_PWRBTN_L (12)
- DBG_RSMRST_L (12)
- DCI_DATA_PTITRACE3_0 (12)
- DBG_PTI_DATA_TRACE3_1 (12)
- DBG_PCH_I2C_SCL (10)
- DBG_PCH_I2C_SDA (10)
- DBG_PTI_DATA_TRACE3_2 (12)
- PCHTX_MIP160RX_UART (10)
- PCHRX_MIP160TX_UART (10)
- DCI_CLK_PTICLK3 (12)

DBG_PMI_RSTBTN_L

C93

*0.01u/16V_2

DBG_PMI_PWRBTN_L

C78

*0.01u/16V_2

*QSH-030-01-L-D-A-K-TR

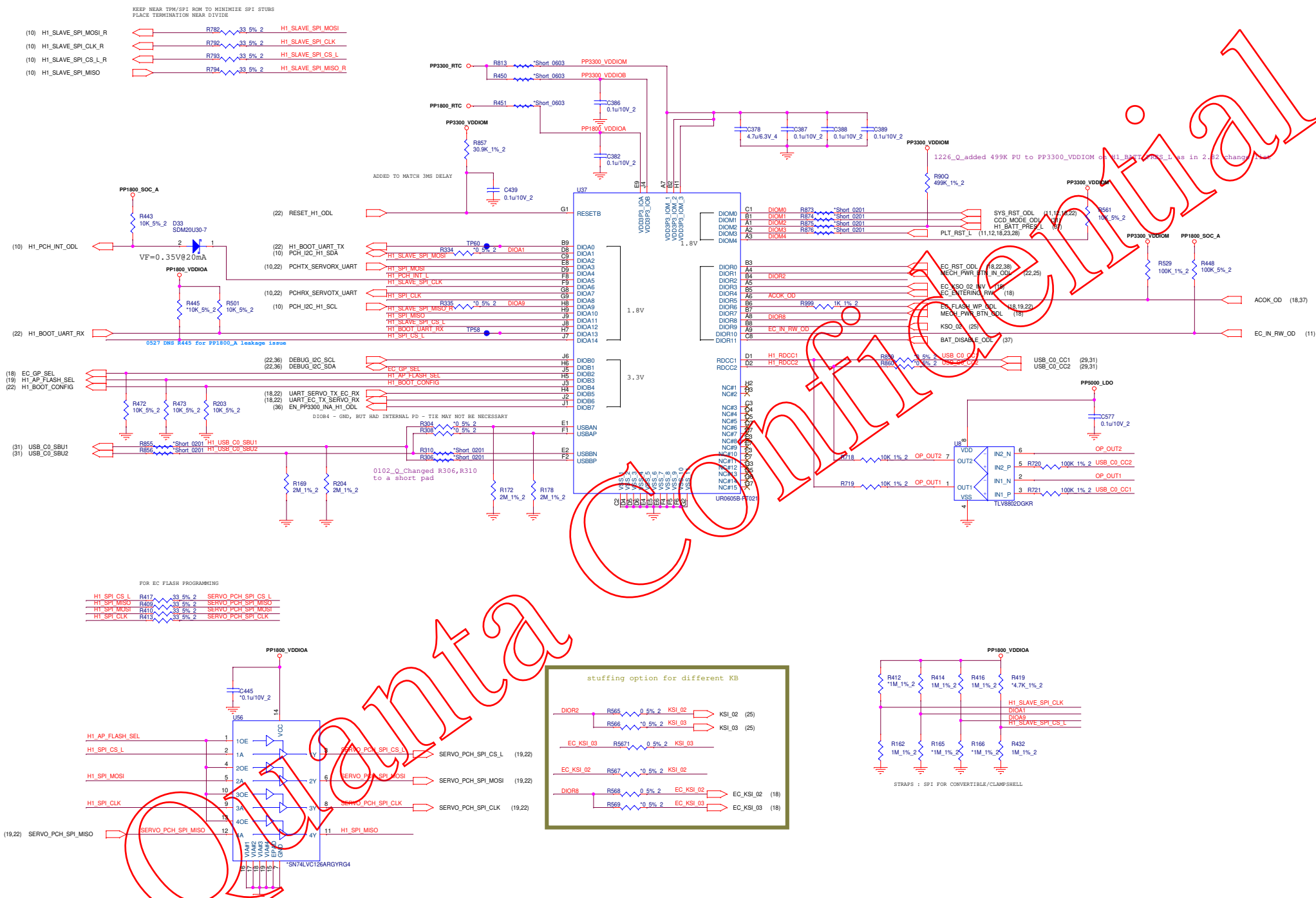


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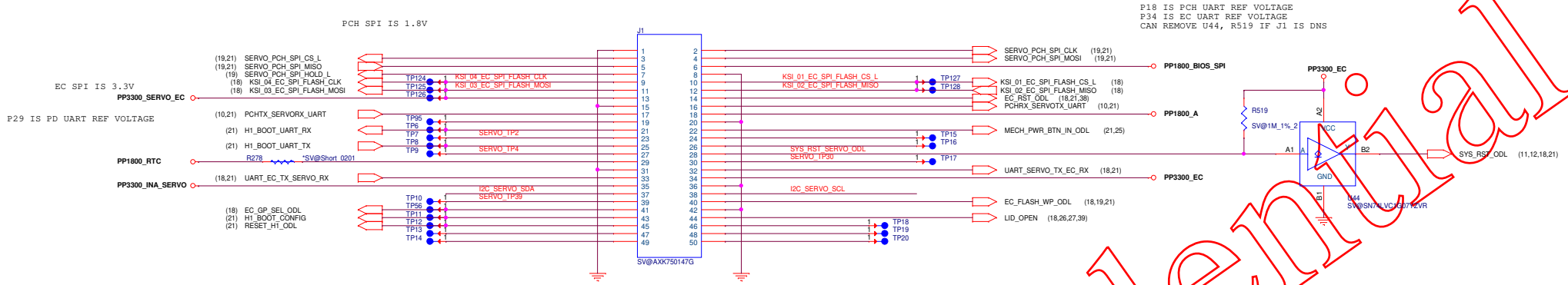
PROJECT : ZAK_ZAN_ZAP_ZAQ

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	MIPI60 DEBUG HEADER	1A
Date:	Thursday, May 30, 2019	Sheet 20 of 45

(H1C)

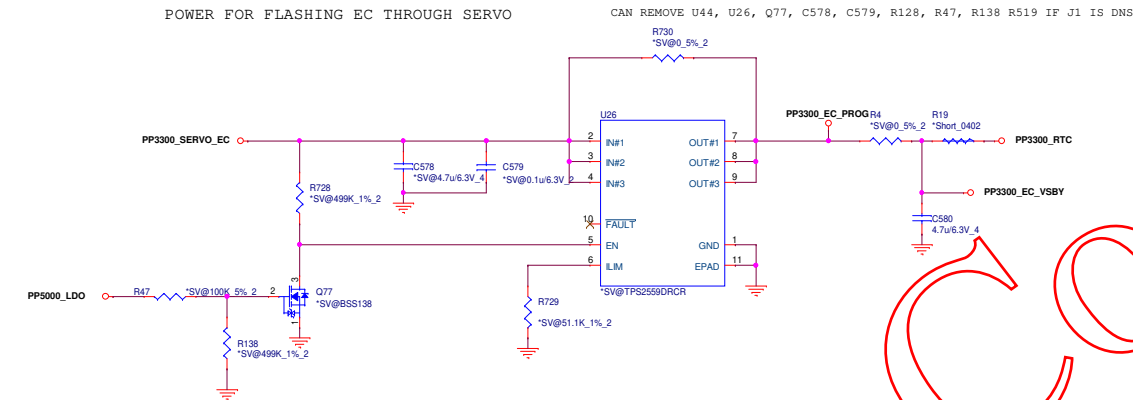


(GOG)

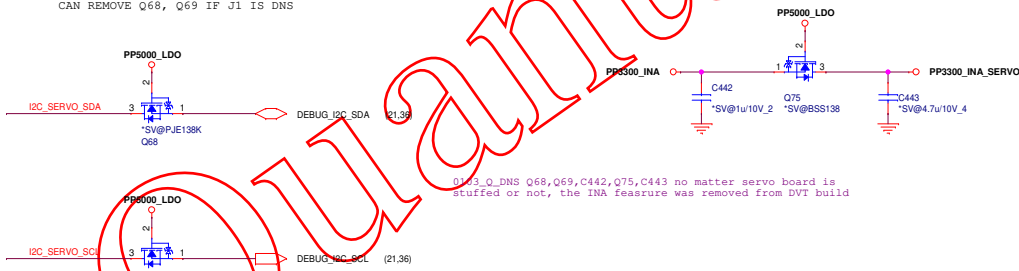


SERVO HEADER

(H1C)

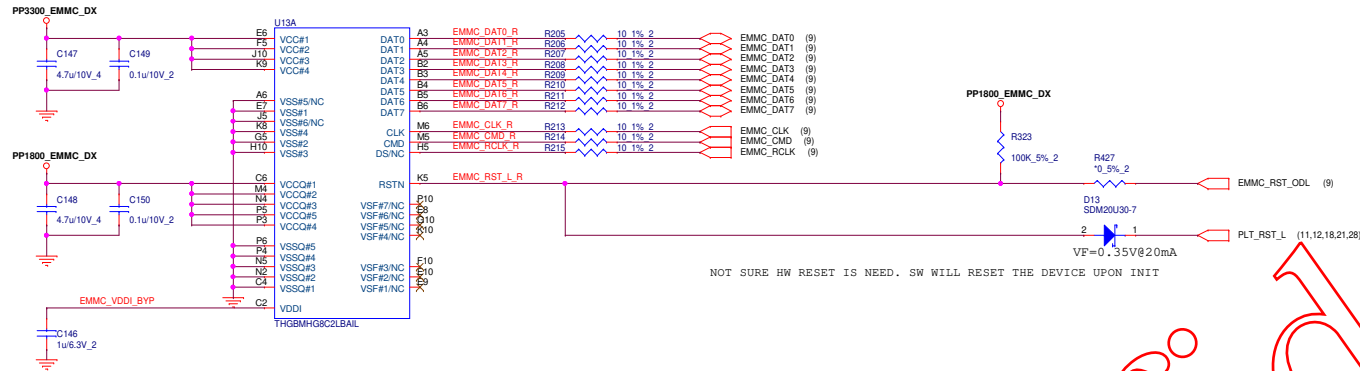


CAN REMOVE Q68, Q69 IF J1 IS DNS



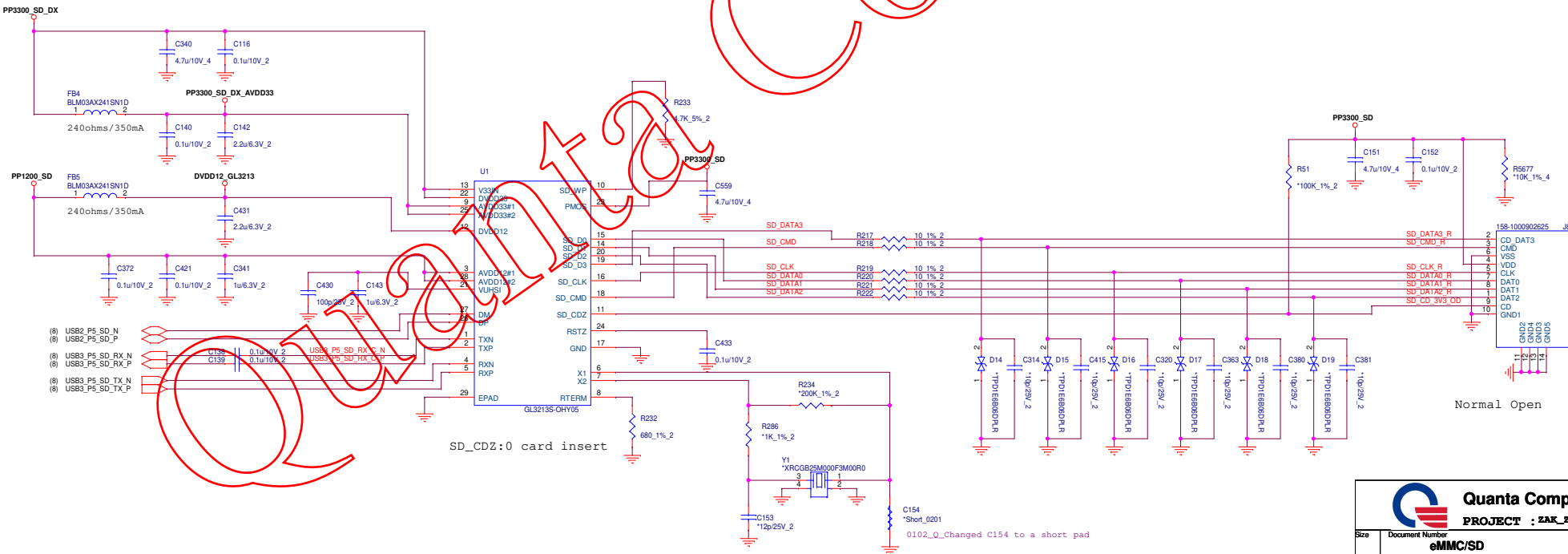
(MMC) 32 GB EMMC STORAGE

150 uA SLEEP CURRENT

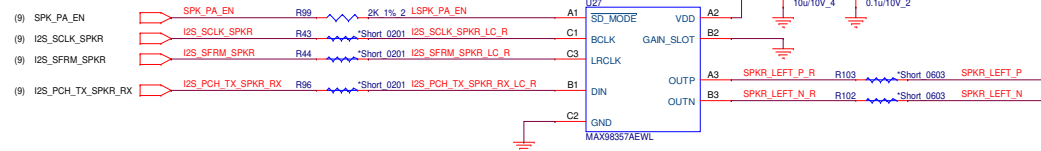


U13B			
A1	NC#A1	NC#H2	H2
A2	NC#A2	NC#H3	H3
A7	RFU#A7/NC	NC#H12	H12
A8	NC#A8	NC#H13	H13
A9	NC#A9	NC#H14	H14
A10	NC#A10	NC#H1	H1
A11	NC#A11	NC#H2	H2
A12	NC#A12	NC#H3	H3
A13	NC#A13	NC#H12	H12
A14	NC#A14	NC#H13	H13
B1	NC#B1	NC#H14	H14
B7	NC#B7	NC#H1	H1
B8	NC#B8	NC#H2	H2
B9	NC#B9	NC#H3	H3
B10	NC#B10	NC#H12	H12
B11	NC#B11	NC#H13	H13
B12	NC#B12	NC#H14	H14
B13	NC#B13	NC#H1	H1
B14	NC#B14	NC#H2	H2
C1	NC#C1	NC#H3	H3
C2	NC#C2	NC#H12	H12
C3	NC#C3	NC#H13	H13
C4	NC#C4	NC#H14	H14
C5	NC#C5	NC#H1	H1
C6	NC#C6	NC#H2	H2
C7	NC#C7	NC#H3	H3
C8	NC#C8	NC#H12	H12
C9	NC#C9	NC#H13	H13
C10	NC#C10	NC#H14	H14
C11	NC#C11	NC#H1	H1
C12	NC#C12	NC#H2	H2
C13	NC#C13	NC#H3	H3
C14	NC#C14	NC#H12	H12
D1	NC#D1	NC#H13	H13
D2	NC#D2	NC#H14	H14
D3	NC#D3	NC#H1	H1
D4	NC#D4	NC#H2	H2
D5	NC#D5	NC#H3	H3
D6	NC#D6	NC#H12	H12
D7	NC#D7	NC#H13	H13
D8	NC#D8	NC#H14	H14
D9	NC#D9	NC#H1	H1
D10	NC#D10	NC#H2	H2
D11	NC#D11	NC#H3	H3
D12	NC#D12	NC#H12	H12
D13	NC#D13	NC#H13	H13
D14	NC#D14	NC#H14	H14
E1	NC#E1	NC#H1	H1
E2	NC#E2	NC#H2	H2
E3	NC#E3	NC#H3	H3
E4	NC#E4	NC#H12	H12
E5	NC#E5	NC#H13	H13
E6	NC#E6	NC#H14	H14
E7	NC#E7	NC#H1	H1
E8	NC#E8	NC#H2	H2
E9	NC#E9	NC#H3	H3
E10	NC#E10	NC#H12	H12
E11	NC#E11	NC#H13	H13
E12	NC#E12	NC#H14	H14
E13	NC#E13	NC#H1	H1
E14	NC#E14	NC#H2	H2
F1	NC#F1	NC#H3	H3
F2	NC#F2	NC#H12	H12
F3	NC#F3	NC#H13	H13
F4	NC#F4	NC#H14	H14
F5	NC#F5	NC#H1	H1
F6	NC#F6	NC#H2	H2
F7	NC#F7	NC#H3	H3
F8	NC#F8	NC#H12	H12
F9	NC#F9	NC#H13	H13
F10	NC#F10	NC#H14	H14
F11	NC#F11	NC#H1	H1
F12	NC#F12	NC#H2	H2
F13	NC#F13	NC#H3	H3
F14	NC#F14	NC#H12	H12
G1	NC#G1	NC#H13	H13
G2	NC#G2	NC#H14	H14
G3	NC#G3	NC#H1	H1
G4	NC#G4	NC#H2	H2
G5	NC#G5	NC#H3	H3
G6	NC#G6	NC#H12	H12
G7	NC#G7	NC#H13	H13
G8	NC#G8	NC#H14	H14
G9	NC#G9	NC#H1	H1
G10	NC#G10	NC#H2	H2
G11	NC#G11	NC#H3	H3
G12	NC#G12	NC#H12	H12
G13	NC#G13	NC#H13	H13
G14	NC#G14	NC#H14	H14
H1	NC#H1	NC#H1	H1

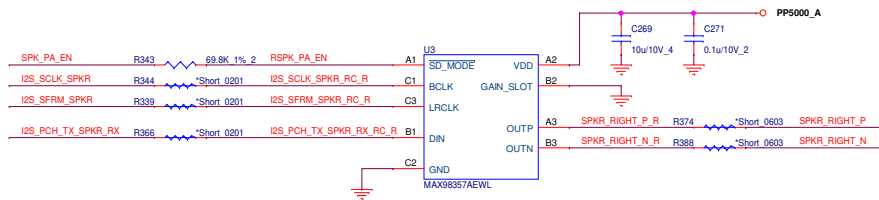
(CRD) MICRO SD CARD



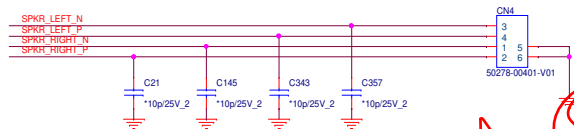
(AMP)



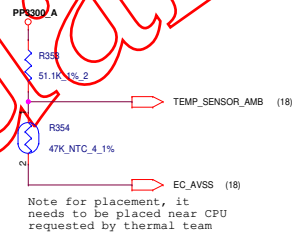
RIGHT CHANNEL



(ADO)

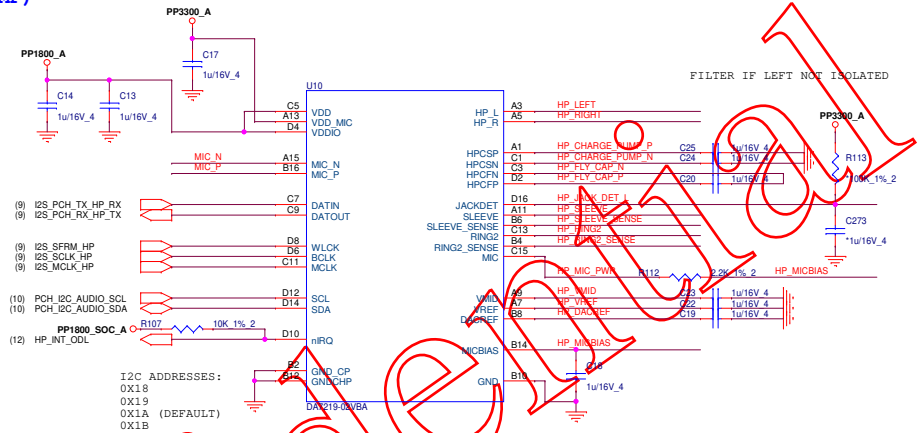


(THM)

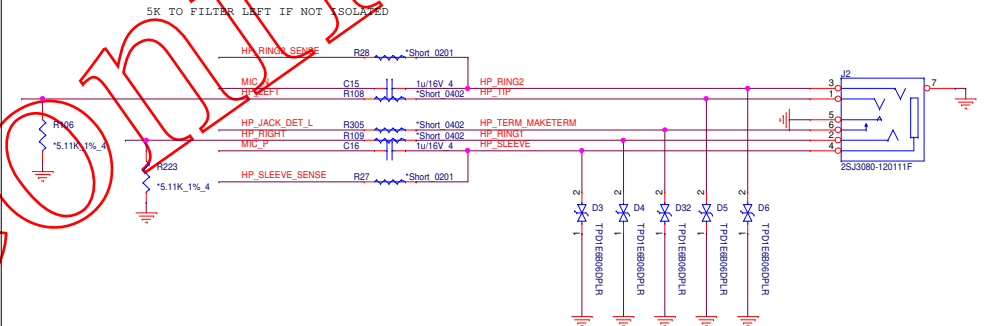


CSP PACKAGE, BUT CAN BE ROUTED ON TYPE-3
<10UA IN DEEP SLEEP

(AMP)



(ADO)



Audio Jack	11" ZBA/ZBB	1st	DFTJ06FRA33
		2nd	DFTJ06FRA54
	14"/15" ZBC/ZBD	1st	DFTJ06FRA44
		2nd	DFTJ06FR985

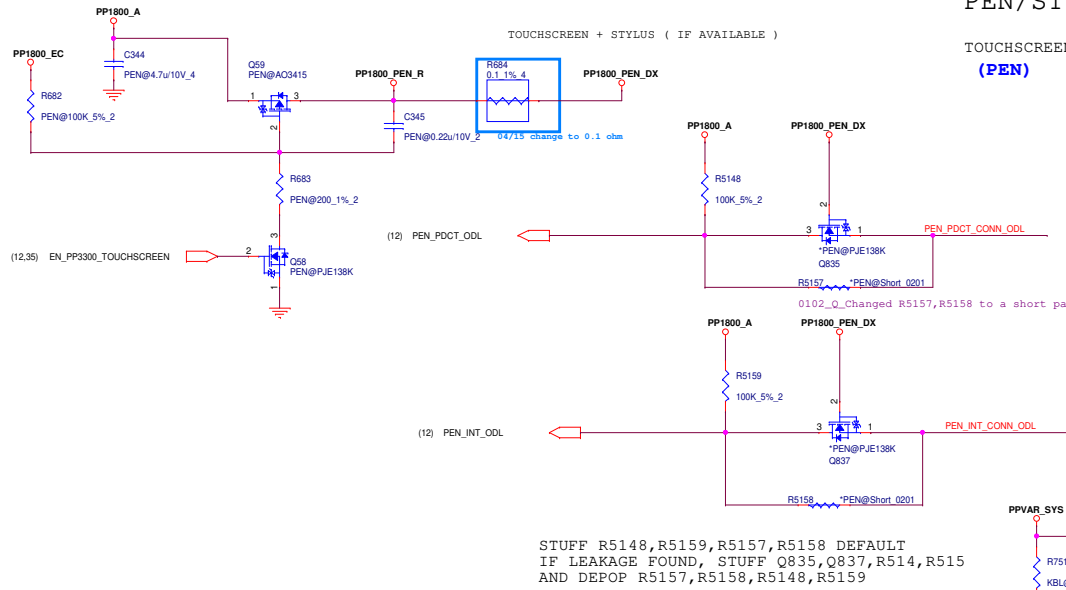
CHANGED MIC SERIES CAPS TO 1UF TO MATCH 10HZ 3DB
FREQUENCY RECOMMENDED IN THE DA7219 DATASHEET

THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL)
THE SAME APPLIES TO HP_SLEEVE AND HP_SLEEVE_SENSE SIGNALS
ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

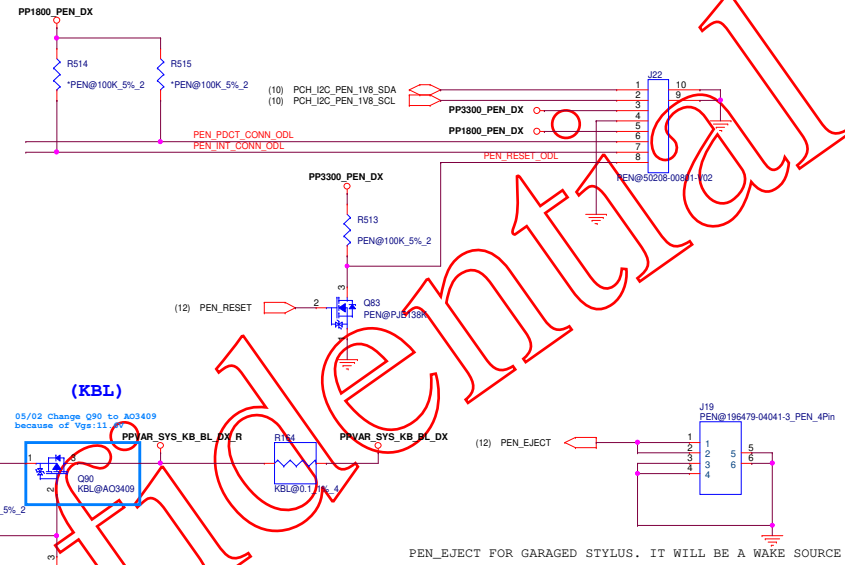
(PEN)

PEN/STYLUS CONNECTOR

PEN 7-BIT I2C ADDRESS = 0X09
~ 100 MA



STUFF R5148,R5159,R5157,R5158 DEFAULT
IF LEAKAGE FOUND, STUFF Q835,Q837,R514,R515
AND DEPOP R5157,R5158,R5148,R5159

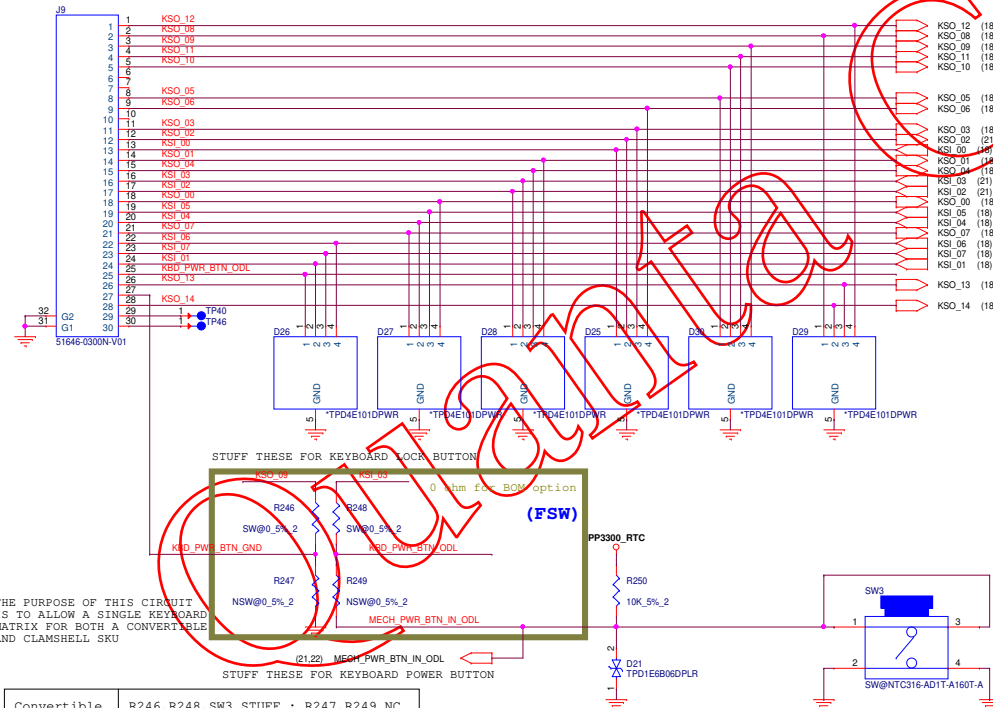


PEN_EJECT FOR GARAGED STYLUS. IT WILL BE A WAKE SOURCE

(KBC)

KEYBOARD

CM TO CHOOSE CONNECTOR- THIS ONE WILL SUPPORT THE KEYPAD SO THE PINOUT MAY NEED TO CHANGE



THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEY
MATRIX FOR BOTH A CONVERT
AND CLAMSHELL SKU

[illegible]

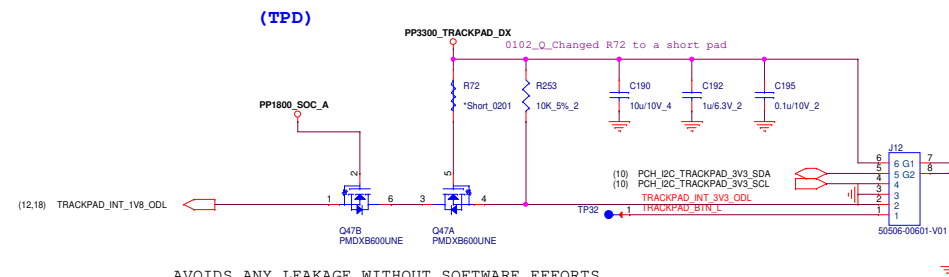
(21,22) MECH_PWR_BTN_IN_ODL

STUFF THESE FOR KEYBOARD POWER BUTTON

Convertible	R246,R248,SW3 STUFF ; R247,R249 NC
Clamshell	R247,R249 STUFF ; R246,R248,SW3 NC

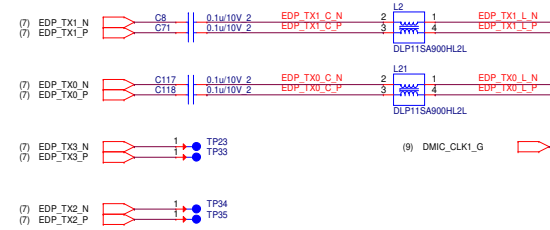
TRACKPAD CONNECTOR

CM TO CHOOSE CONNECTOR



AVOIDS ANY LEAKAGE WITHOUT SOFTWARE EFFORTS

EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR

[illegible]

PP1800_SENSOR_U

C108
GS@4.7u10V_4

C109
GS@0.1u6.3V_2

PP1800_SENSOR_U

(18) LID_ACCEL_INT_L
(18,27) EC_I2C_SENSOR_U_SDA
(18,27) EC_I2C_SENSOR_U_SCL

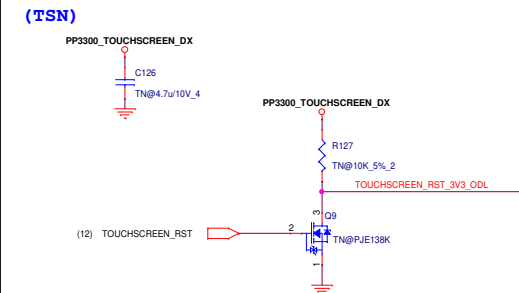
1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

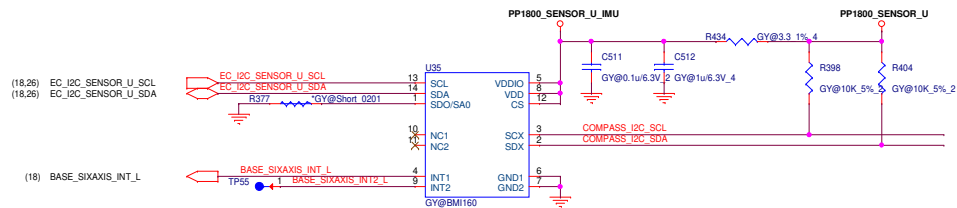
GS@500208-00501-V02

~~WFC CAMERA~~

WFC INTERFACE PINOUT TBD. PENDING CHANGE



(GRS)



IMU

MODE 2 (SLAVE TO EC, MASTER TO MAG)
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 7'0X68 (LSB SET BY SD0/SA0) -->8'0XD0h

(ACM)

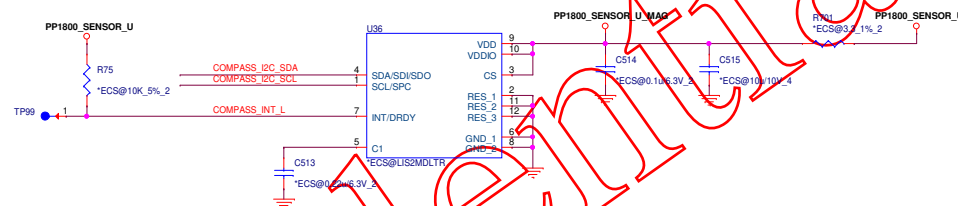
0 ohm for BOM option

R30Q~R32Q place near to IMU U35

EC_I2C_SENSOR_U_SCL R30Q *ACM@0 5% 2
EC_I2C_SENSOR_U_SDA R31Q *ACM@0 5% 2
BASE_SIXAXIS_INT_L R32Q *ACM@0 5% 2

for AR Camera, IMU can be DNS, but R30Q,R31Q,R32Q need to be stuffed

(ECS)



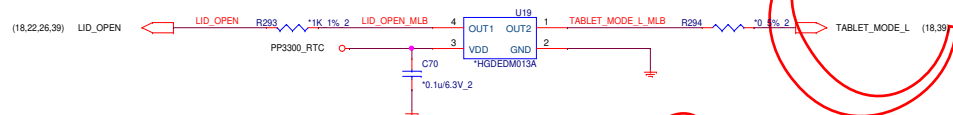
MAGNETOMETER

SLAVE TO IMU SENSOR
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 0X1E

GMR SENSOR (RESERVED FOR ON BOARD SITUATION)

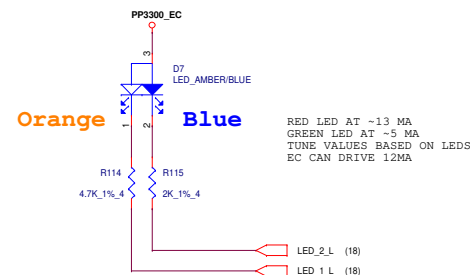
(UIF)

(GMR_MLB) For on board GMR



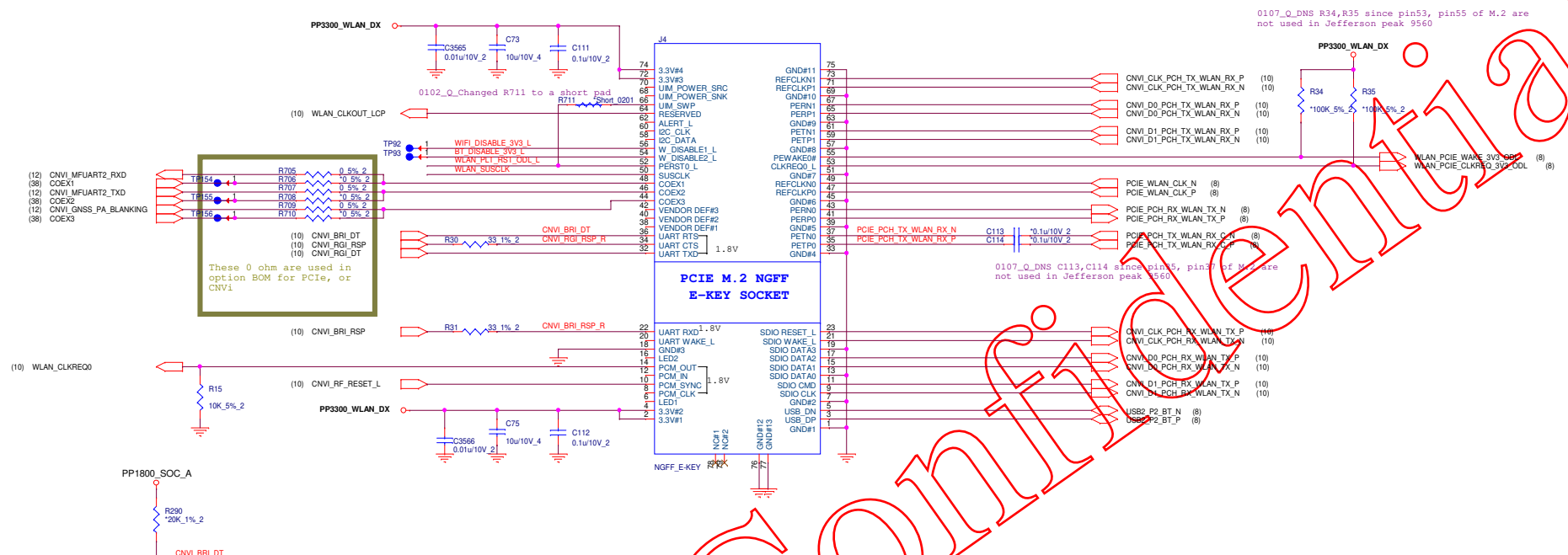
MAKE SURE TO CHECK THE POLARITY OF MAGNET TO ASSIGN THE PIN LID-OPEN AND TABLET-MODE
IF THE GMR SENSOR IS NOT PLACED ON THE MLB, PLEASE CAREFULLY PLAN THE PINOUT ON THE SUB-BOARD INTERFACE.

CHARGE/BATTERY LED

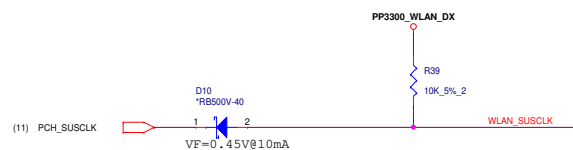
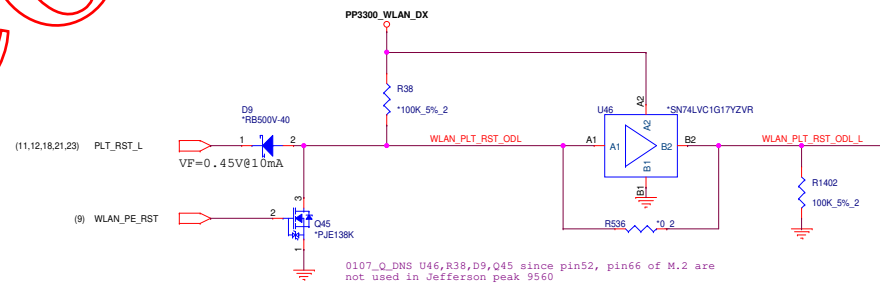
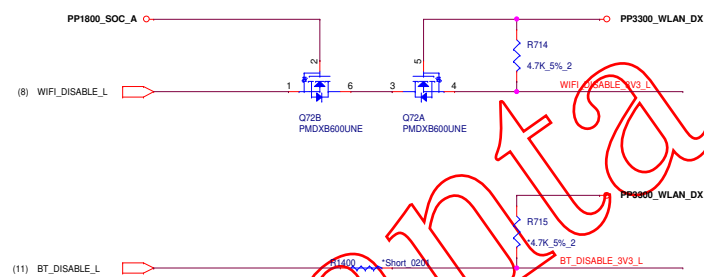


CM TO CHOOSE CONNECTOR

(NGF)



PLACE THE PULL-UP R CLOSE TO M.2. (FOR DEBUG)



U46,R38,D9,Q45,C113,C114,R34,R35,Q1,Q2 need to be stuffed for WiFi flexible design

(UTC1)

FOR USB-C PORT 0

TO MLB CONNECTOR

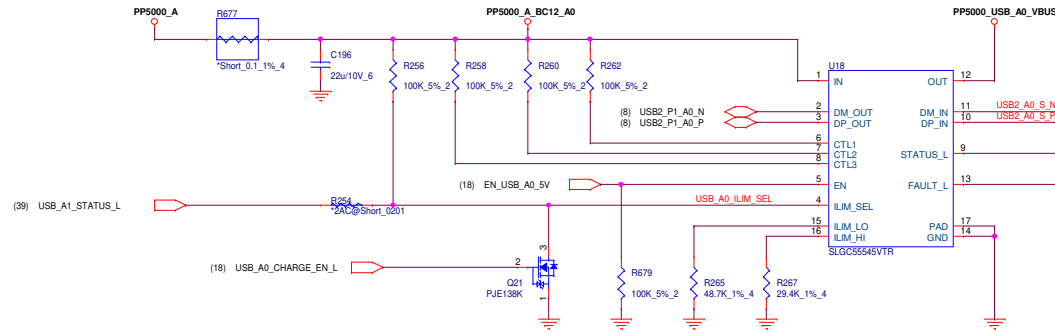
leave USB_C0_DISCHARGE/EN_USB_C0_5V_3A_ILIM
NC and keep components being stuffed for
debug purpose

WITH THE NX20P3483, THE VBUS DISCHARGE CAN BE SW CONTROL

USB_C0_PD_RST IS ACTIVE HIGH WITH 100K INTERNAL PD

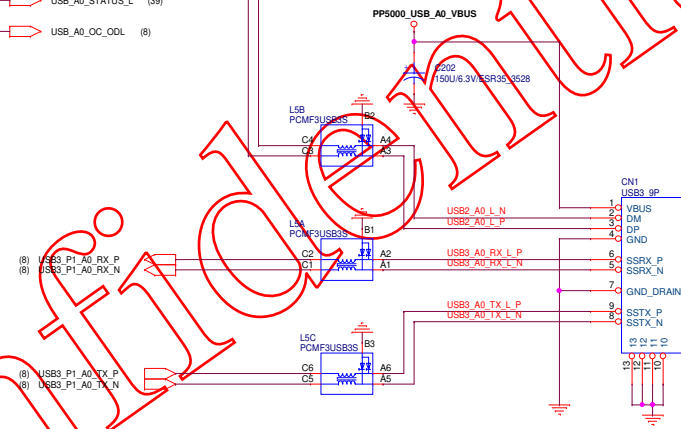
BC 1.2 FOR THE TYPE-A PORT A0

(UBC1)



(UB31)

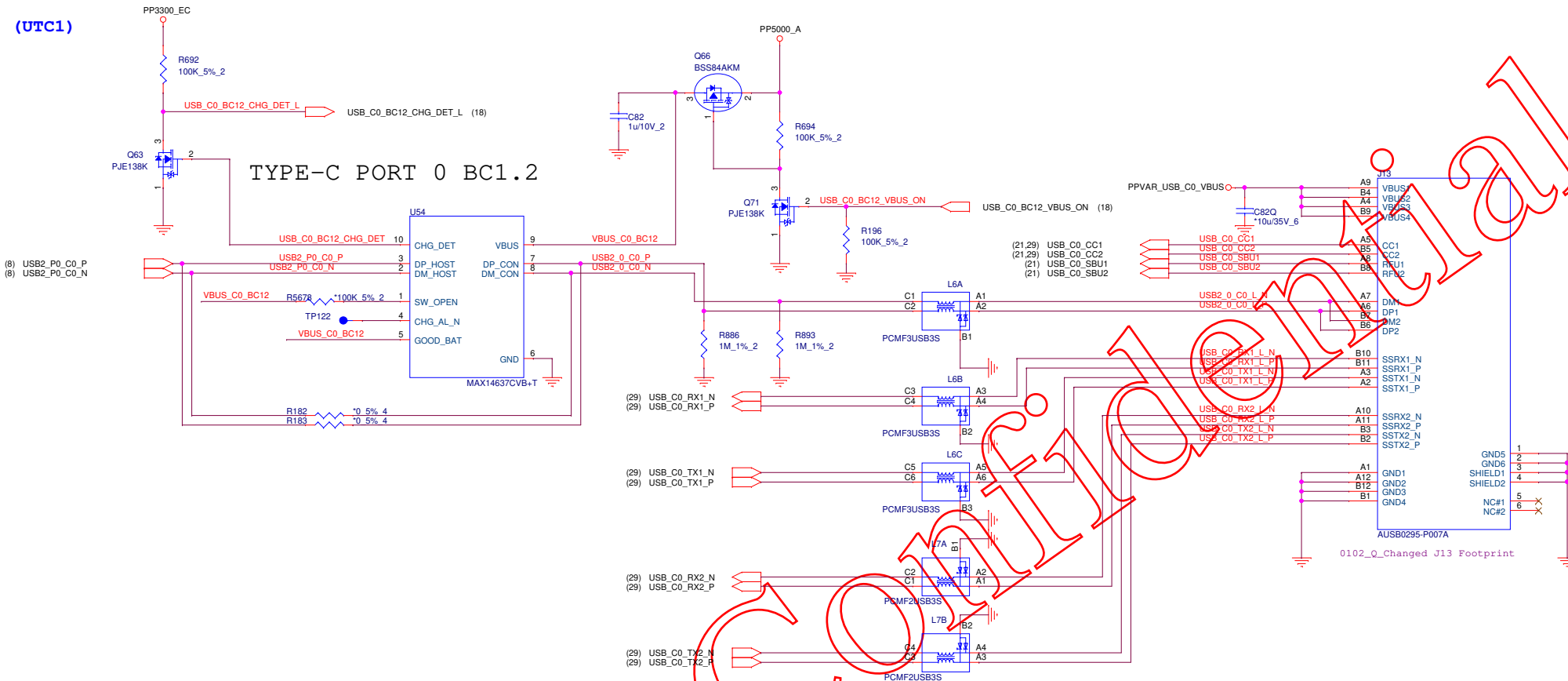
CM TO CHOOSE CONNECTOR



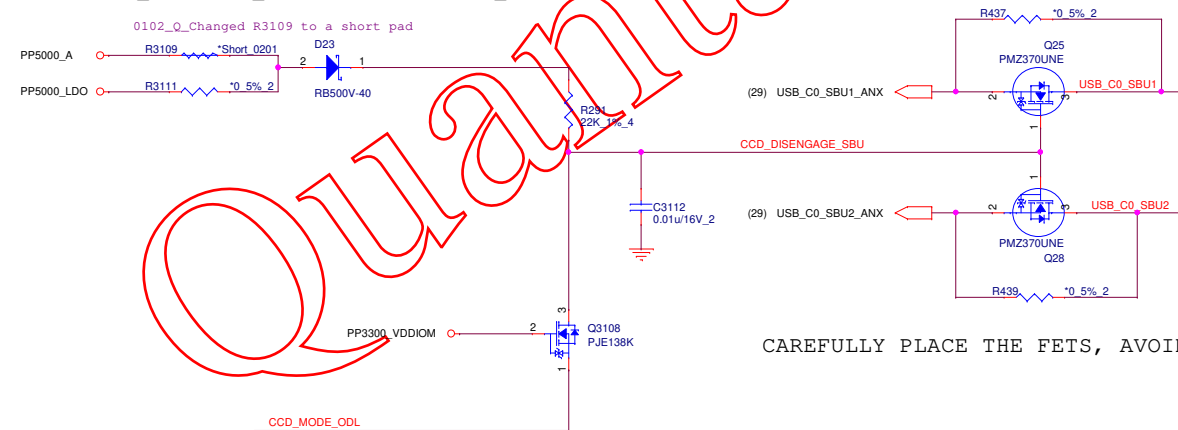
USB3.0 Type-A conn	11" ZBA/ZBB	1st	DFHS09FR780
		2nd	DFHS09FR790
	14" ZBC	1st	DFHS09FR937
		2nd	DFHS09FR936
	15" ZBD	1st	DFHS09FRB05
		2nd	DFHS09FRB06
		3rd	DFHS09FRB07

(UTC1)

TYPE-C PORT 0 BC1.2

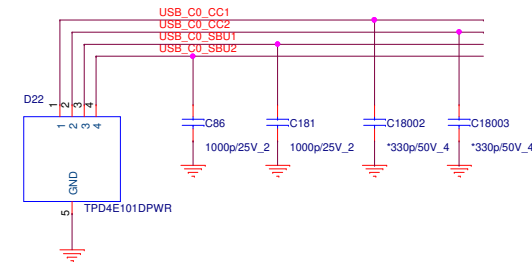


ONLY TIME CCD_DISENGAGE_SBU IS HIGH WHEN CCD_MODE IS INACTIVE AN THERE IS POWER TO THE TCPC



CAREFULLY PLACE THE FETS, AVOID LONG STUB

(UTC1)

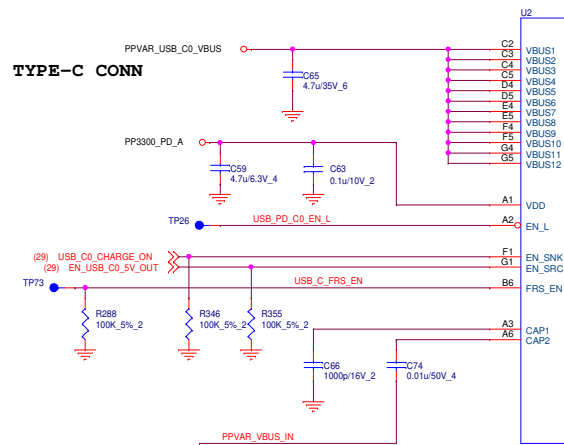


(PUB1)

PORT 0

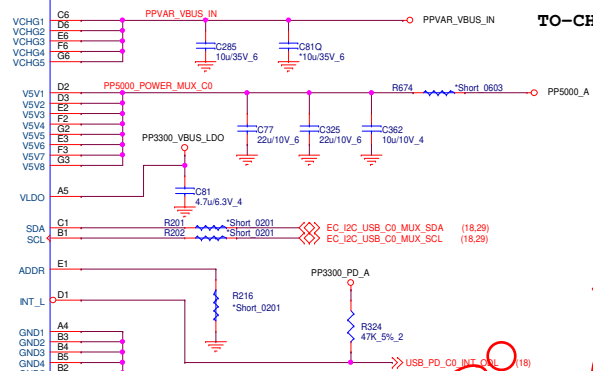
PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR

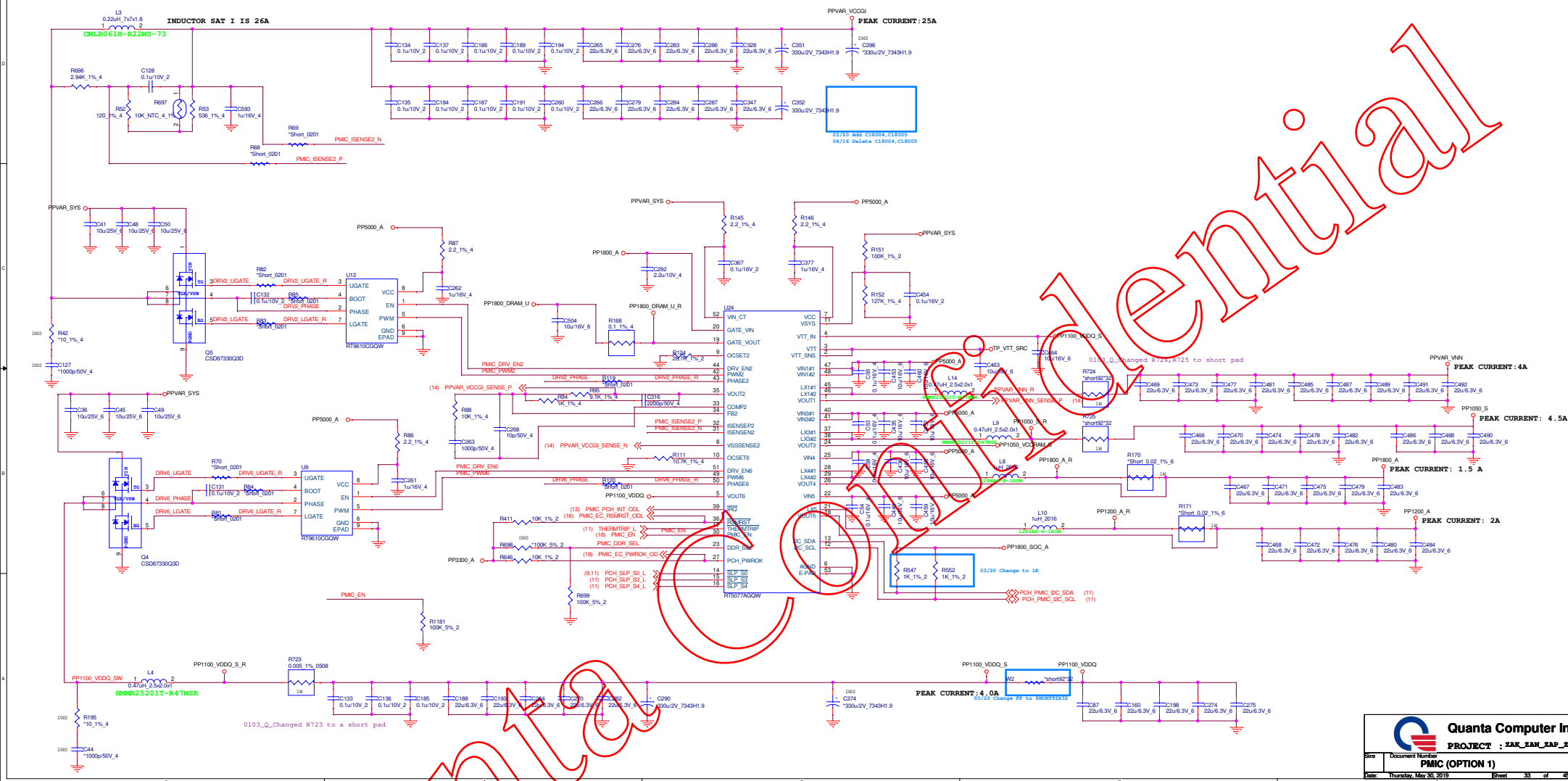
TYPE-C CONN



NX20P3483

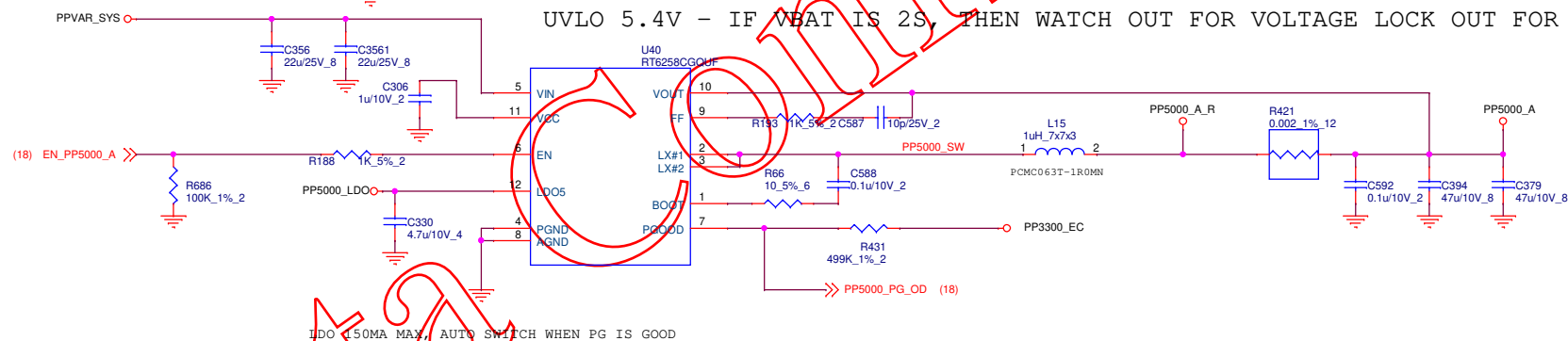
TO-CHARGER





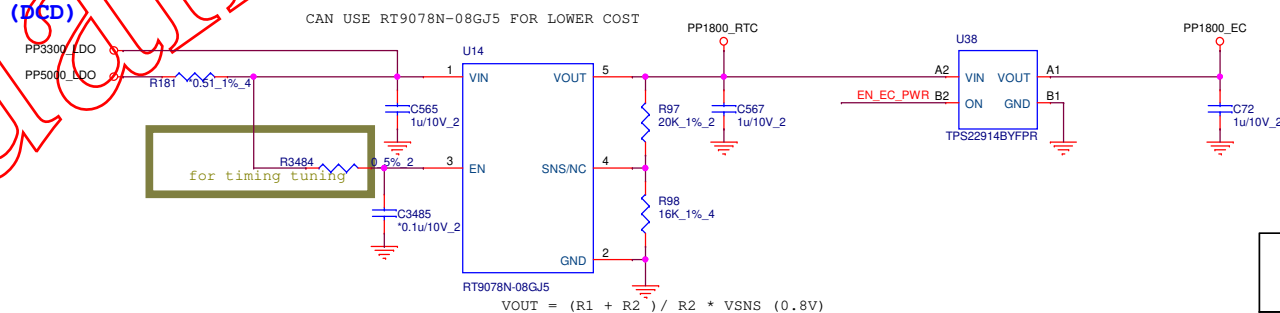


UVLO 5.4V - IF VBAT IS 2S, THEN WATCH OUT FOR VOLTAGE LOCK OUT FOR 1.8V

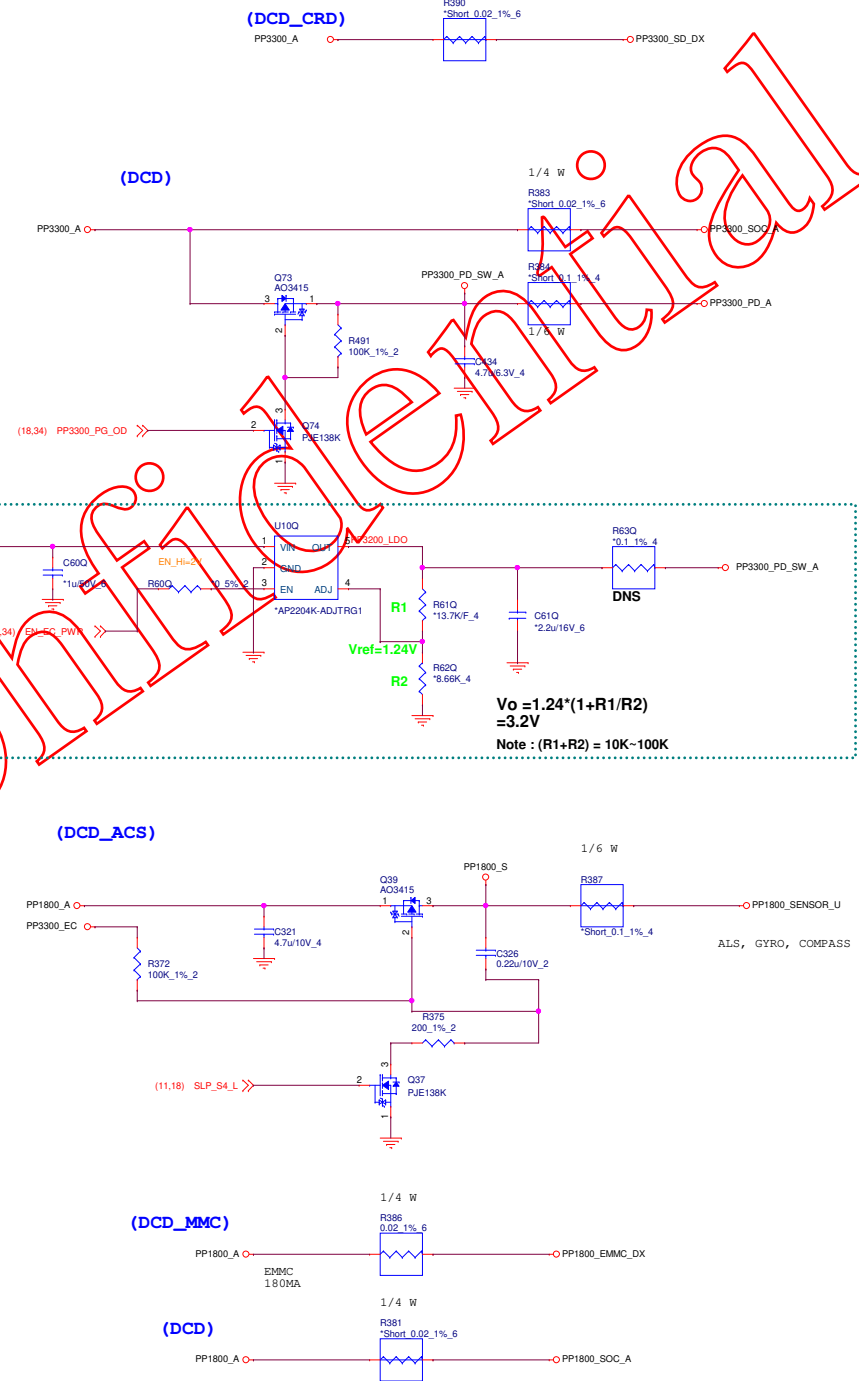


PP1800_RTC CAN BE GENERATED BY A SEPARATE DC-DC R
CAN USE RT9078N-08GJ5 FOR LOWER COST

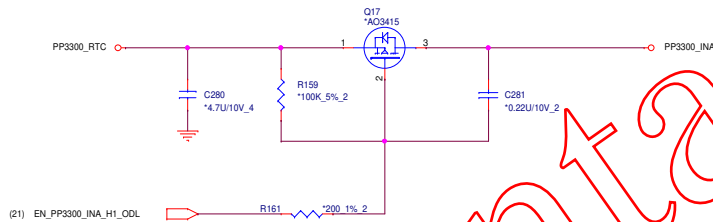
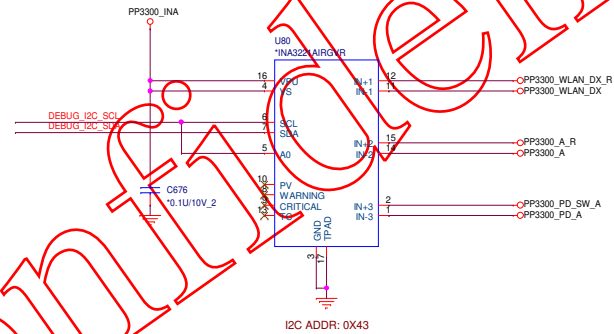
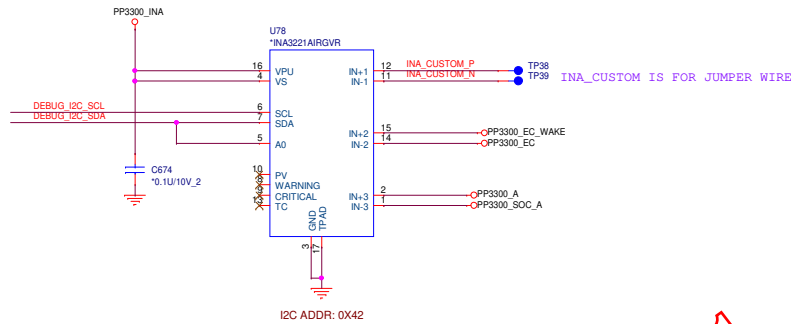
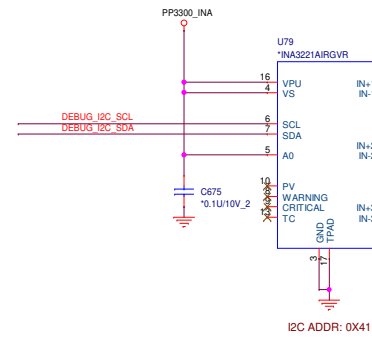
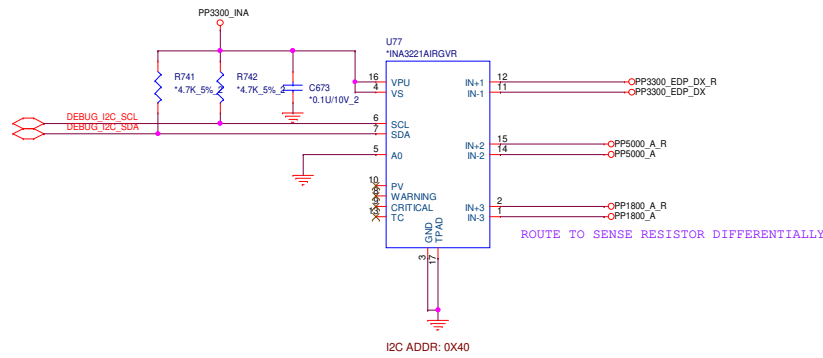
PP1800_EC CAN BE GENERATED BY A SEPARATE REGULATOR


$$V_{OUT} = (R_1 + R_2) / R_2 * V_{SNS} \quad (0.8V)$$

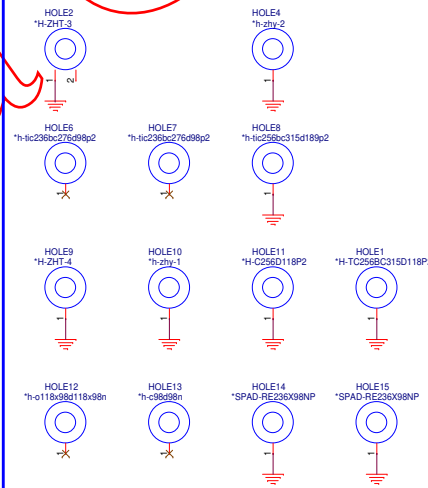
CHOICES FOR THE REGULATORS CAN BE SUBSTITUE AFTER CONFIRM THE FUNCTIONALITY.



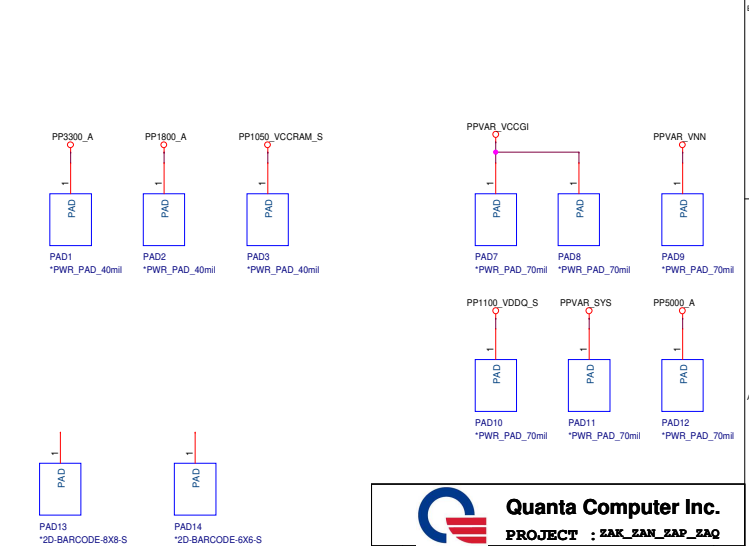
(INA)



HOLES (OTH)



POWER TEST PAD (OTH)



INTERSIL BUCK - BOOST CHARGER

INCREASE OR ADD POSCAPS IF AUDIBLE NOISE IS HEARD

RECOMMENDED VALUE
FROM DATASHEET

RECOMMENDED VALUE
FROM DATASHEET

REQUIRE HIGHER
OUTPUT CAPACITANCE

RATING
HIGH ENOUGH?

0102_Q_removed R475,R476,R477 used as 0 ohm in
EVT/DVT builds for layout optimization

BATGONE LOW
INDICATES
BATTERY PRESENT

FOR 0.476A ADAPTER CURRENT LIMIT
AND 733KHz SWITCHING FREQUENCY:
2CELL : 93.1K
3CELL : 105K

I2C ADDR : 0X12

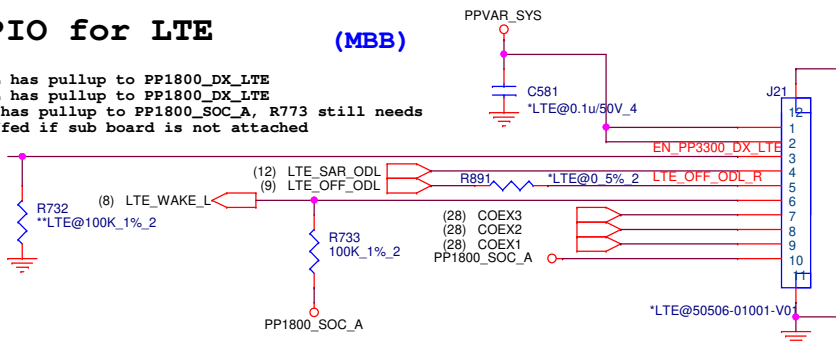
CV: 12.6V
3S1P Battery

GPIO for LTE

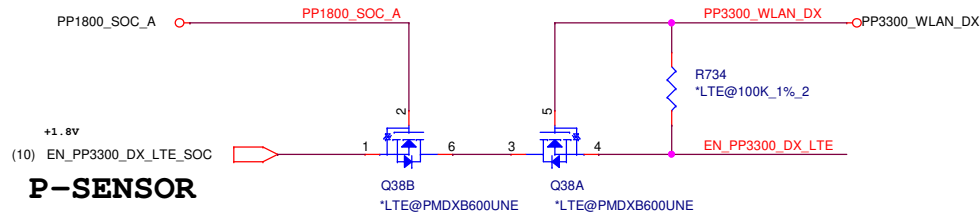
(MBB)

Coral sub board

- LTE_SAR_ODL has pullup to PP1800_DX_LTE
- LTE_OFF_ODL has pullup to PP1800_DX_LTE
- LTE_WAKE_L has pullup to PP1800_SOC_A, R773 still needs to be stuffed if sub board is not attached

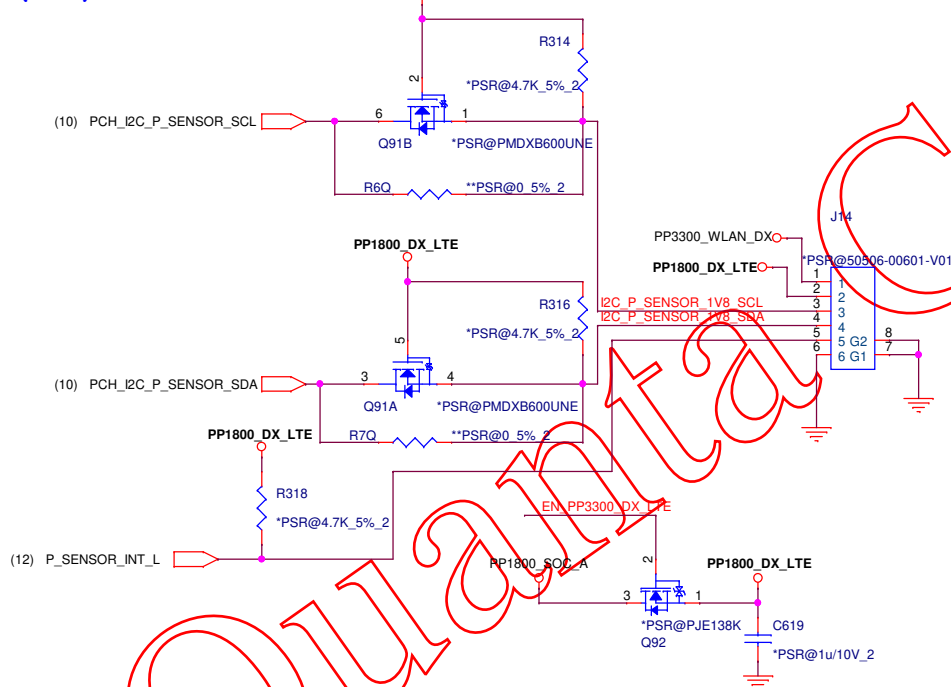


LEVERAGING CORAL BOARD!



P-SENSOR

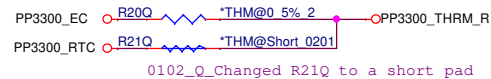
(PXS)



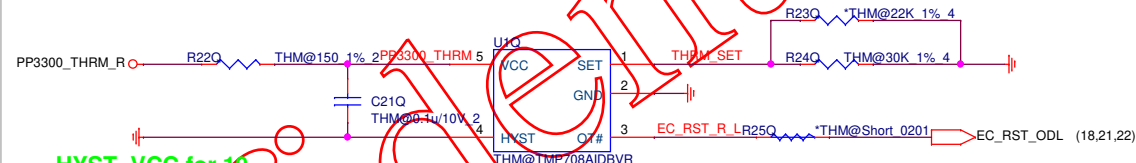
(SYS_THM)

Thermal Protector

Need fine tune
for thermal protect point
Note placement position
TEMP=76.3C



$$R_{set}(Kohm) = 0.0012T^*T - 0.9308T + 96.147$$



HYST=VCC for 10
degree Hys.
HYST=GND for 30
degree Hys.

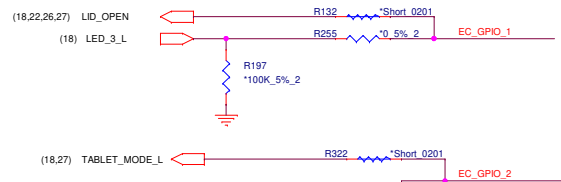


Quanta Computer Inc.

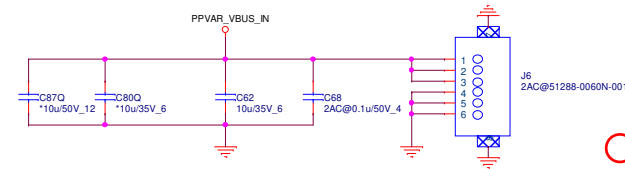
PROJECT : ZAK_ZAN_ZAP_ZAQ

Size	Document Number	Rev
	LTE\$TEST	1A
Date:	Thursday, May 30, 2019	Sheet 38 of 45

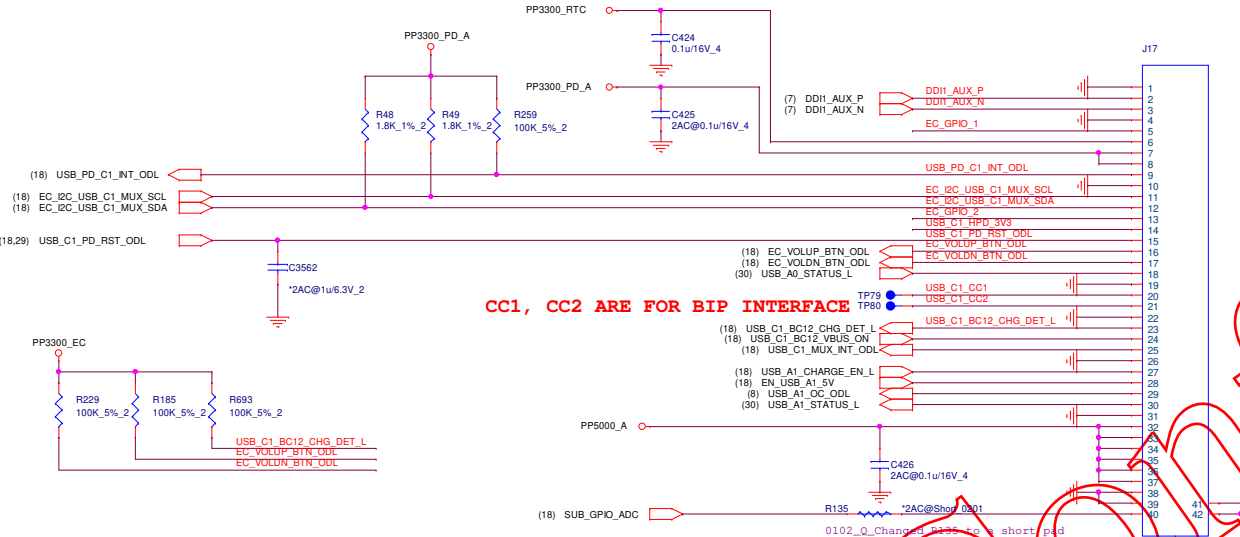
(UTC2)



EC_GPIO1,2 CAN BE USED FOR CONNECTING THE GMR SENSOR ON THE SUB-BOARD
OR IT CAN BE USED TO CONNECT AN SPARE EC GPIO PINS FOR ADDITIONAL CONTROL FROM EC



PULL-DOWN RESISTORS TO AVOID
FLOATING INPUT W/O SUB-BOARD



CC1, CC2 ARE FOR BIP INTERFACE

SUB_GPIO_ADC GOES TO AN ADC PIN OF EC WITH STUFFING OPTIONS
THE PIN CAN BE USED FOR VBUS DETECT OR FOR BOARD ID DETECT, OR USE AS A GENERAL GPIO FROM EC

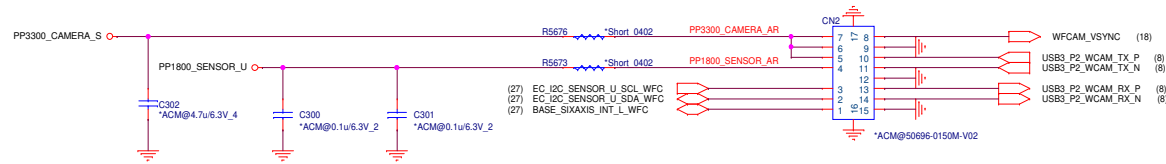
SELECT PER SEL SI TEAM
CM TO ADJUST PINOUT/PIN COUNT

- (8) USB3_P4_C1_TX_P
- (8) USB3_P4_C1_TX_N
- (8) USB2_P3_A1_N
- (8) USB2_P3_A1_P
- (8) USB3_P4_C1_RX_P
- (8) USB3_P4_C1_RX_N
- (8) USB2_P4_C1_P
- (8) USB2_P4_C1_N
- (7) DDH1_TX3_N
- (7) DDH1_TX3_P
- (7) DDH1_TX2_N
- (7) DDH1_TX2_P
- (7) DDH1_TX1_N
- (7) DDH1_TX1_P
- (7) DDH1_TX0_N
- (7) DDH1_TX0_P
- (8) USB3_P3_A1_RX_N
- (8) USB3_P3_A1_RX_P

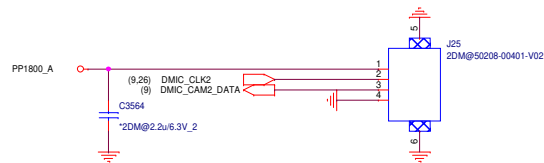
SELECT PER SEL SI TEAM

MOTHER BOARD INTERFACE

AR CAMERA CONN (ACM)



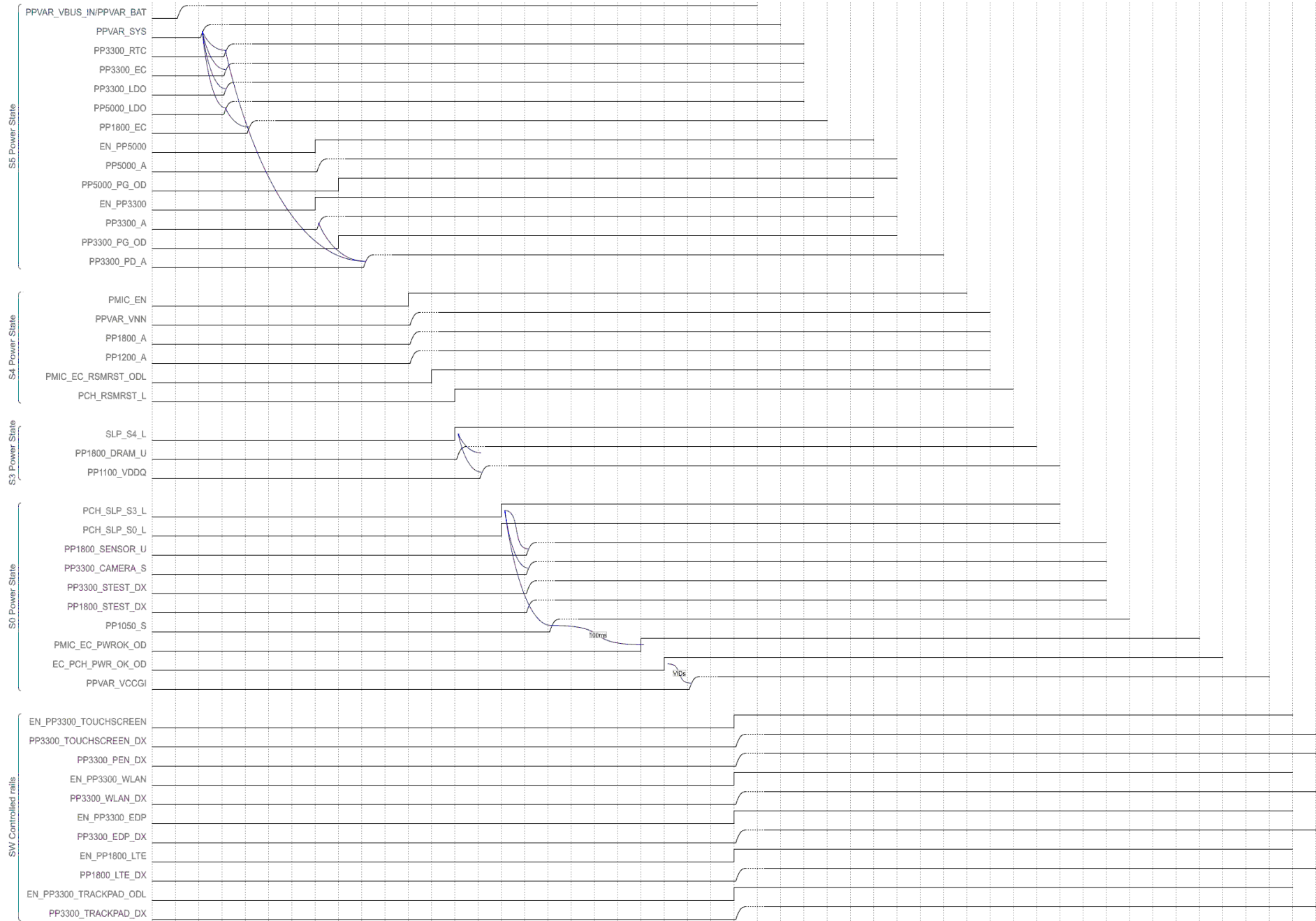
DMIC CONN (MIC2)



PREFERRED DMIC CHANNEL CONFIG
INTERFACE 1: STRAP MIC TO LEFT=CHANNEL 0
INTERFACE 2: STRAP MIC TO RIGHT=CHANNEL 3

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GPIO #	Bump Name	Voltage	Bootstrap Termination	Default Termination	Bootstrap Purpose	Bootstrap Usage	Bootstrap	Octopus Signal Name
GPIO_27	GPIO_27	1.8V	20K PU	20K PD	eMMC as boot Source 20K PU internal	1 = enable (default) 0 = disable	eMMC Boot	DBG_PTI_DATA_16
GPIO_28	GPIO_28	1.8V	20K PU	20K PD	SPI as boot Source 20K PU internal	1 = enable (default) 0 = disable	SPI Boot	DBG_PTI_DATA_17
GPIO_42	GP_INTD_DS1_TE1	1.8V	20K PD	20K PD	Flash Descriptor Override for SPI security features	1 = Override 0 = No Override (default)	Flash Descriptor	TP_WIFI_RST_N, TP135
GPIO_43	GP_INTD_DS1_TE2	1.8V	20K PU	20K PD	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GP_INTD_DS1_TE2
GPIO_44	USB_OC0_B	1.8V	20K PD	20K PU	RVSD	1 = Do Not Use 0 = disable (default)	RSVD	USB_A_OC_ODL
GPIO_45	USB_OC1_B	1.8V	20K PD	20K PU	Top Swap Override. Have core look for BIOS code in SPI ROM	1 = Enable 0 = disable (default)	Top Swap	USB_C_OC_ODL
GPIO_61	LPSS_UART0_TXD	1.8V	20K PD	20K PU	TXE to bypass ROM in SoC and go to patch space	1 = enable bypass 0 = disable (default)	TXE ROM Bypass	PCHTX_MIP160RX_UART
GPIO_62	LPSS_UART0_RTS	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_INT_L
GPIO_65	LPSS_UART2_TXD	1.8V	20K PD	20K PU	TXE to perform DnX for new FW Image over USB.	1 = Force DnX 0 = Do Not Force (default)	DnX FW Load	PCHTX_UART2
GPIO_66	LPSS_UART2_RTS	1.8V	20K PD	20K PU	LPC Boot BIOS strap	1 = LPC Boot 0 = No LPC Boot (default)	LPC Boot	LTE_OFF_ODL
GPIO_79	LPSS_SPI_0_CLK	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	H1_SLAVE_SPI_CLK_R
GPIO_80	LPSS_SPI_0_FSD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = No halt (default)	RSVD	H1_SLAVE_SPI_CS_L_R
GPIO_81	LPSS_SPI_0_FS1	1.8V	20K PU	20K PU	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GPIO_81_DEBUG (Boot halt)
GPIO_83	LPSS_SPI_0_TXD	1.8V	20K PD	20K PD	Sets the LPC buffer to 1.8V or 3.3V mode	1 = 1.8V mode 0 = 3.3V mode (default)	LPC Voltage Select	H1_SLAVE_SPI_MOSI_R
GPIO_84	LPSS_SPI_2_CLK	1.8V	20K PU	20K PD	SPI Boot BIOS Strap	1 = Don't SPI Boot (default) 0 = SPI Boot Debug if Secure boot fuse is set to 0	SPI Boot Source	stest_SPI1_CLK_R
GPIO_85	LPSS_SPI_2_FSD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_SPI_CS_L_R
GPIO_86	LPSS_SPI_2_FS1	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = enable (default)	RSVD	stest_CNTRL
GPIO_87	LPSS_SPI_2_FS2	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	TP_PCH_GPIO_87_PD
GPIO_89	LPSS_SPI_2_TXD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	stest_SPI1_MOSI_R
GPIO_159	AVS_I2S0_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	I2S0_PCH_RX
GPIO_163	AVS_I2S1_WS_SYN	1.8V	20K PD	20K PD	SMBus 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	Buffers 1.8V/3.3V	I2S_SFRM_5PKR
GPIO_164	AVS_I2S1_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	WLAN_PE_RST
GPIO_168	AVS_HDA_SDI	1.8V	20K PD	20K PD	PMU 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	PMU 1.8V/3.3V	I2S2_PCH_RX
GPIO_172	AVS_M_CLK_B1	1.8V	20K PD	20K PD	SMBus No Reboot. Handled by PMC	1 = Enable 0 = disable (default)	SMBus Reboot	DMIC_CLK2_R
GPIO_174	AVS_M_CLK_AB2	1.8V	20K PD	20K PD	VDD2 Voltage Select	1 = 1.24V 0 = 1.20V (default)	VDD2 Voltage	(Open, TP_GPIO_174)
GPIO_175	AVS_M_DATA_2	1.8V	20K PD	20K PD	eSPI vs. LPC	1 = eSPI mode 0 = LPC mode (default)	eSPI/LPC mode	DMIC_CAM2_DATA
GPIO_177	SMB_CLK	1.8V/3.3V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	(Open, TP160)
GPIO_191	CNV_BRI_DT	1.8V	20K PD	None	eSPI Flash Sharing Mode. Set to 0 if GPIO_175 is set to 0	1 = Slave attached Share 0 = Master attached (default)	Flash Sharing	CNV1_BRI_DT_R
GPIO_192	CNV_BRI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNV1_BRI_RSP
GPIO_193	CNV_RGI_DT	1.8V	20K PU	None	RSVD	1 = Normal Operation 0 = Do not use	RSVD	CNV1_RGI_DT_R
GPIO_194	CNV_RGI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNV1_RGI_RSP
GPIO_195	CNV_RF_RESET_B	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNV1_RF_RESET_L
GPIO_196	XTAL_CLKREQ	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	(Not available)